The Hana 1 Soft Core Forth Processor

Silesian University of Technology

SVFIG April 2024

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Mikroinformatyka Systemów

Cyfrowych

Katowice 2024

Stack Machine Motivation

Python, Java, Mozilla Javascript, Postscript and others are all stack based langauges.

Operation	Stack effect	Forth CPU	Arm C

+	(x1 x2 -- sum)	+
		1 clock Cycle
			LDM pt2nd!, {r0}
			ADD pstop, r0, pstop
			2 instructions, 3 cycles

Swap	(x1 x2 – x2 x1)	Swap
		1 clock cycle
			LDR r0, [PT2ND]
			STR PSTOP, [PT2ND]
			MOV PSTOP, r0
			3 instructions, 5 clock cycles

Rotate3	(x1 x2 x3 –
	X3 X1 X2)
		Rot3
		1 clock cycle
			LDM pt2nd!, {r0, r1}
			STMDB pt2nd1 {r1, PSTOP}
			MOV PSTOP, r0
			3 instructions, 7 clock cycles

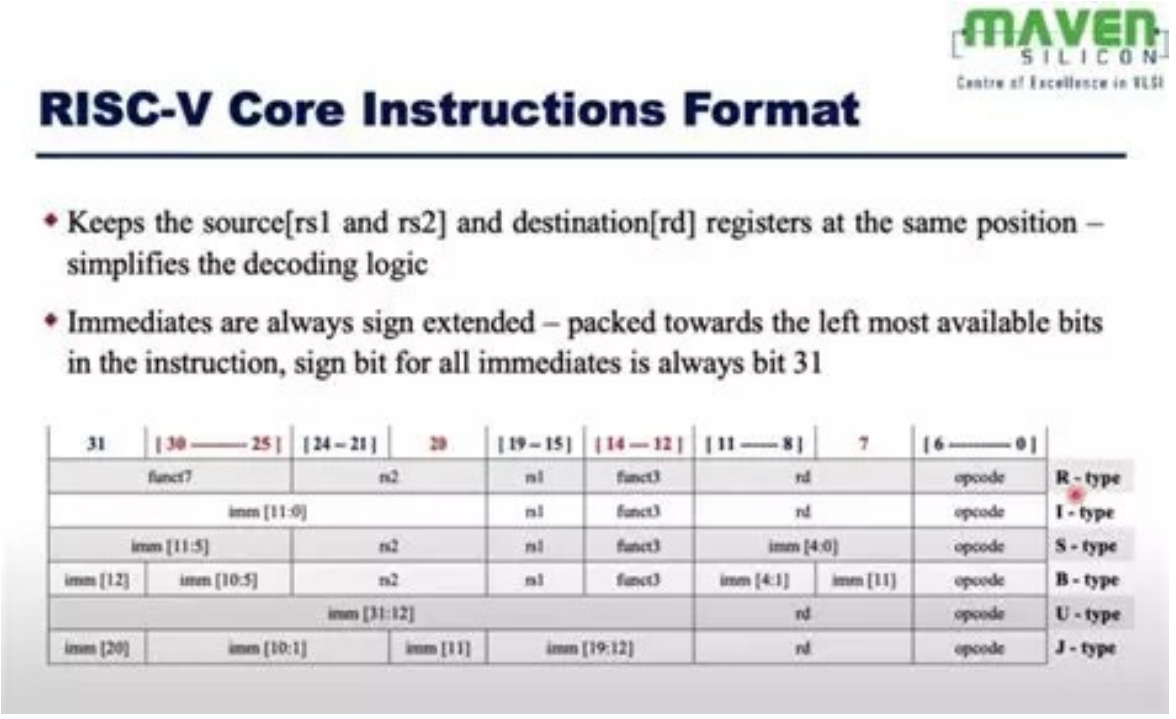
Elided Words

	dup	**over**
+	2dup+	over+
-	2dup-	
xor	2dupxor	overxor
and	2dupand	overand
or	2dupor	overor
=	2dup=	over=
<	2dup<	over>
u<	2dupu<	overu>
>r	2dup>r	
um*low	2dupum*low	
um*high	2dupum*high	
lshift		overswaplshift
rshift		overswaprishift
arshift		overswaparshift

Space and Performance

MicroPython's minimum requirements 256KB of ROM and 16KB of RAM.	Mecrisp fits into 11 kbits of flash or fram and runs with at least 512 bytes of ram.
The Lua interpreter takes 282KB and the Lua library takes 470KB.	Mecrisp fits into 11 kbits of flash or fram and runs with at least 512 bytes of ram.
ZPU 442 Luts.	J1 160 LUTS with a barrel shifter, 80 LUTS with 1 bit shifter.
J1 Video application on Microblaze in C 16380 Bytes	J1 Video application on J1 in Forth. 6349 Bytes

Risc-V Instruction Set



Z = x + y

32 Registers.

5 bits x register

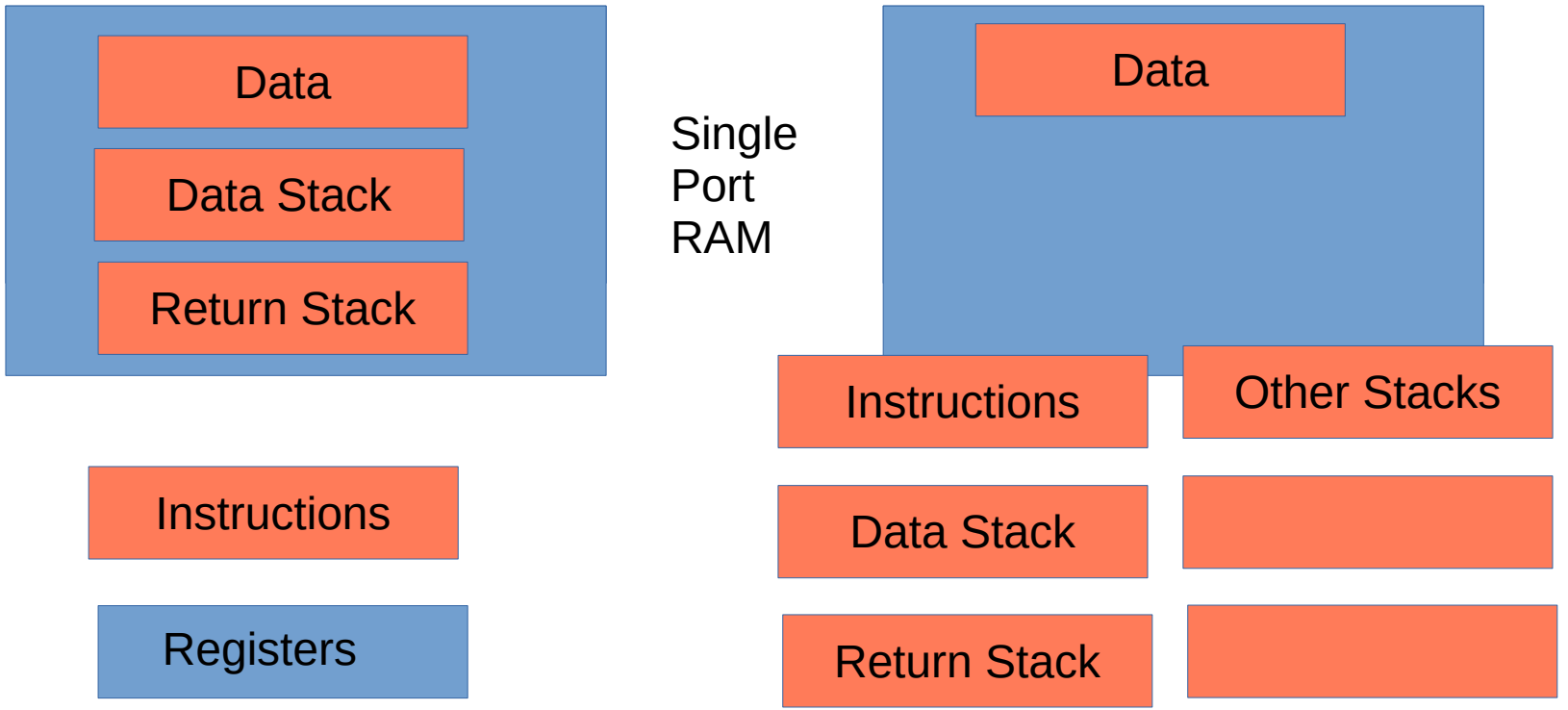
5 bits y register

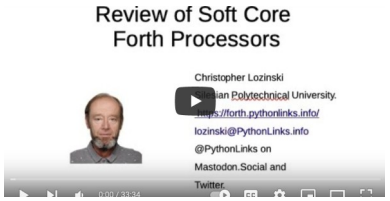
5 bits z register

7 bits Op Code

Less Memory Contention

- Register Machine (C) Stack Machine (Forth)

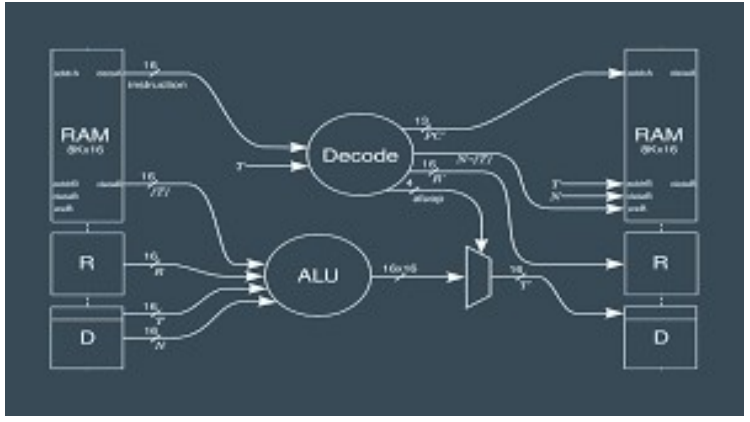




66 Known Forth Soft Cores

	Min Cost	RAM Limits	Min LUTs	Max Speed	Max Memory Efficiency	Max Application Speed	Port-ability	Min Work	Max Design Flexibility
J1	✓		✓	✓					
Mecrisp								✓	
Micro-Core		✓				✓			
EP16…					✓		✓		
J1Sc									✓
Core-1							✓	✓	
Hana-1	✓	✓			✓				
b16	✓				✓			✓	

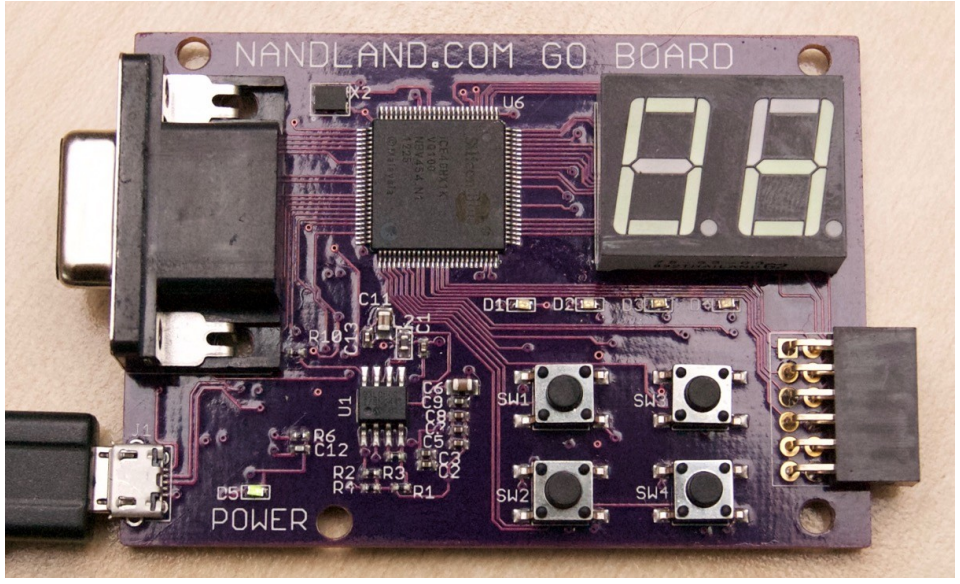
The J1 limitations



No interrupts
No Timer
No Forth
Only 16 instructions
Only 8K Memory addresses
Requires dual port RAM.

Easy to use: Mecrisp-ICE

Enhanced version of Swapforth and the J1a



27 instructions	Nicely commented
16 I/o Ports	Nice Variable names
SPI Flash	Constant folding
gForth	Tail call optimizations
14 supported boards	inlining
Tick counter	PSRAM

The J1 Family of Forth Processors

Default is 16 bits.

J4a

H1 VHDL

J1Sc Scala

J1a PSD RAM

Mecrisp PSD RAM

1

James Bowman J1

Mecrisp Dual Port

2

3 Single Port

Many Core

CSP CPU

Barrel CPU

J1b 32

Mecrisp 32

Mecrisp 64

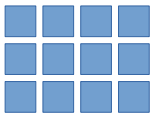
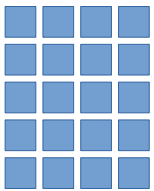
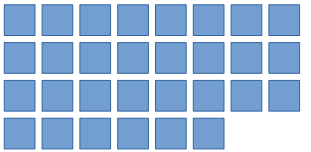
Only Some Versions Shown

FPGA RAM Types

Single Port: One read or write per clock cycle

Dual Port: Two ports can both either read or write during one clock cycle.

Pseudo Dual Port: One port can read, while one port can write during one clock cycle

OLD ICE40LP-1k	NEW ICE40UP5K
 3K App Words  5K System Words Pseudo dual port 32 * 4kbits = 128Kbits PSRAM 8k * 16 bit words.	 30 * 4kbits = 120Kbits of PSRAM 10**14bits Single Port 10**14bits Single Port 10**14bits Single Port 10**14bits Single Port 4* 16Kbits = 1MBit SPRAM

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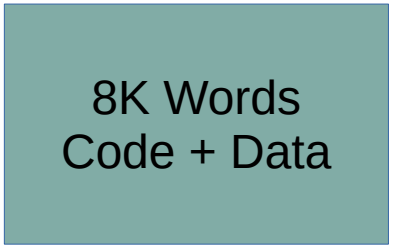
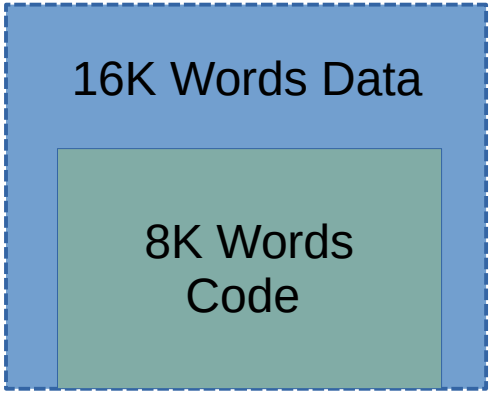
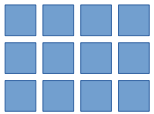
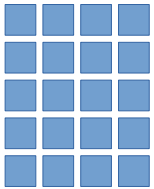
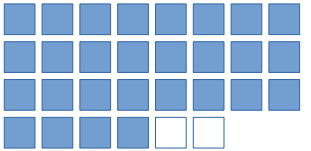
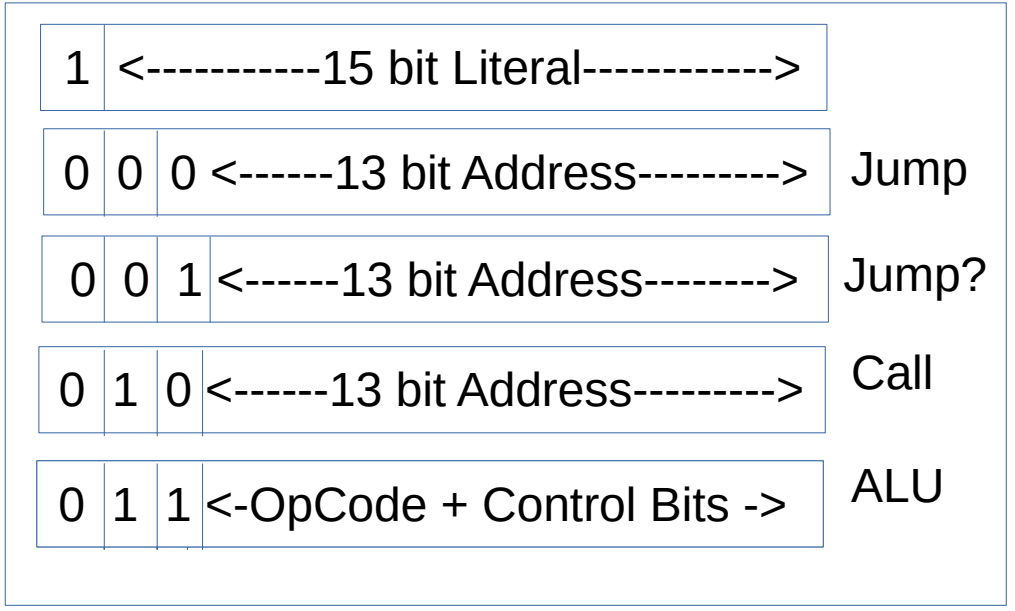
Mecrisp Vs Hana 1

	Mecrisp Ice 16bit PSRAM	Hana 1 16 bit SPRAM
4Kbit PSRAM	30	2
LUTs	2141/ 5280	~1006s=
Max Frequency	17.45 Mhz	23.12 MHz
Flexibility	Poor	Excellent
Memory Model		
Free Memory		26 Brams 3 SPRAMS

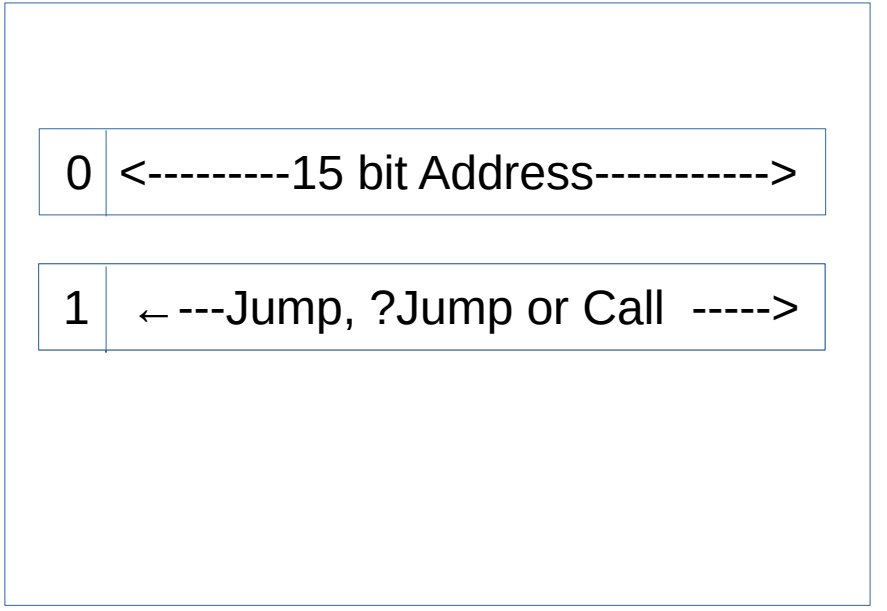
OLD ICE40LP-1k	NEW ICE40UP5K
 3K App Words  5K System Words Pseudo dual port 32 * 4kbits = 128Kbits PSRAM 8k * 16 bit words.	 30 * 4kbits = 120Kbits of PSRAM 10**14bits Single Port 10**14bits Single Port 10**14bits Single Port 10**14bits Single Port 4* 16Kbits = 1MBit SPRAM

16 Bit Jump Instructions

J1 Instruction Set

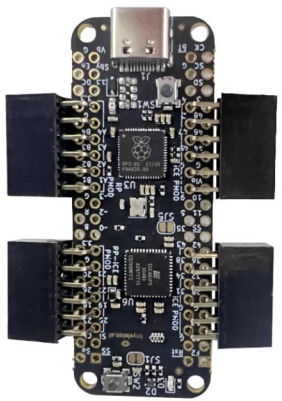


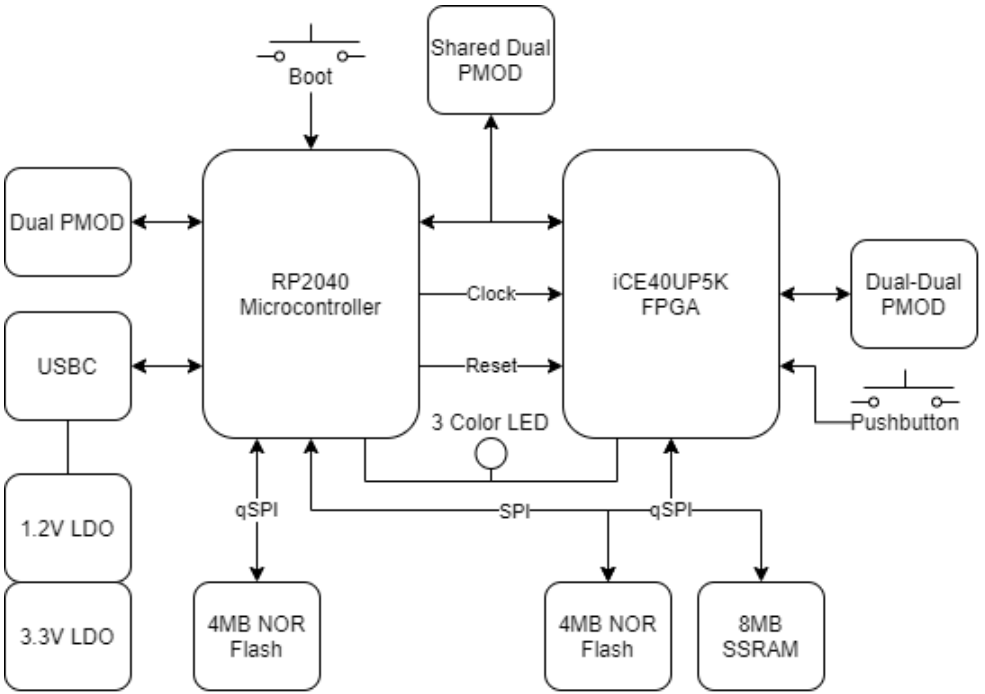
Mainstream Forth Cores



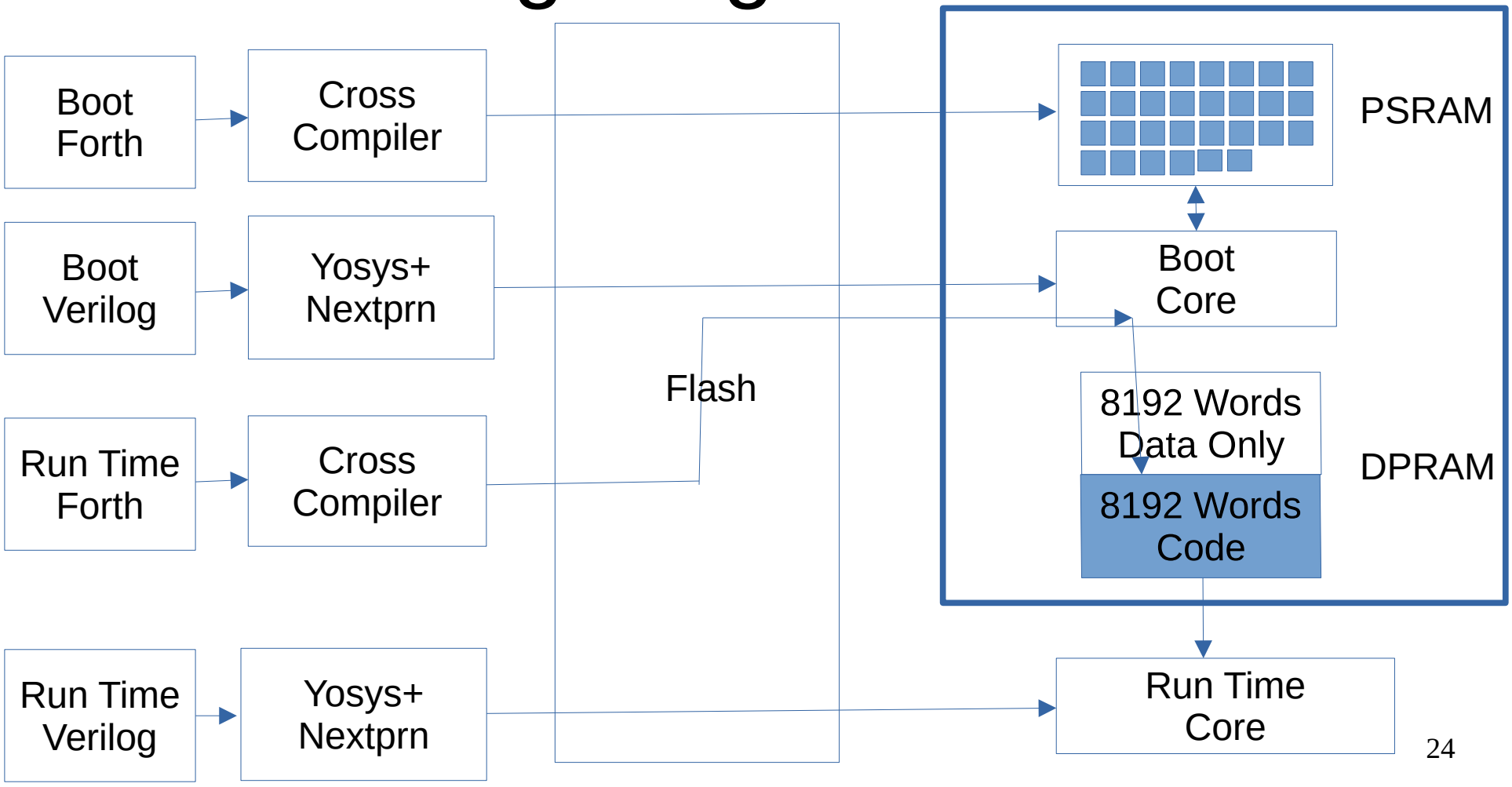
D. Gregg, M. A. Ertl, and J. Waldron, "The Common Case in ForthPrograms," in EuroForth, 2001.

Open Source Pico-Ice Hardware





Initializing Single Port RAM



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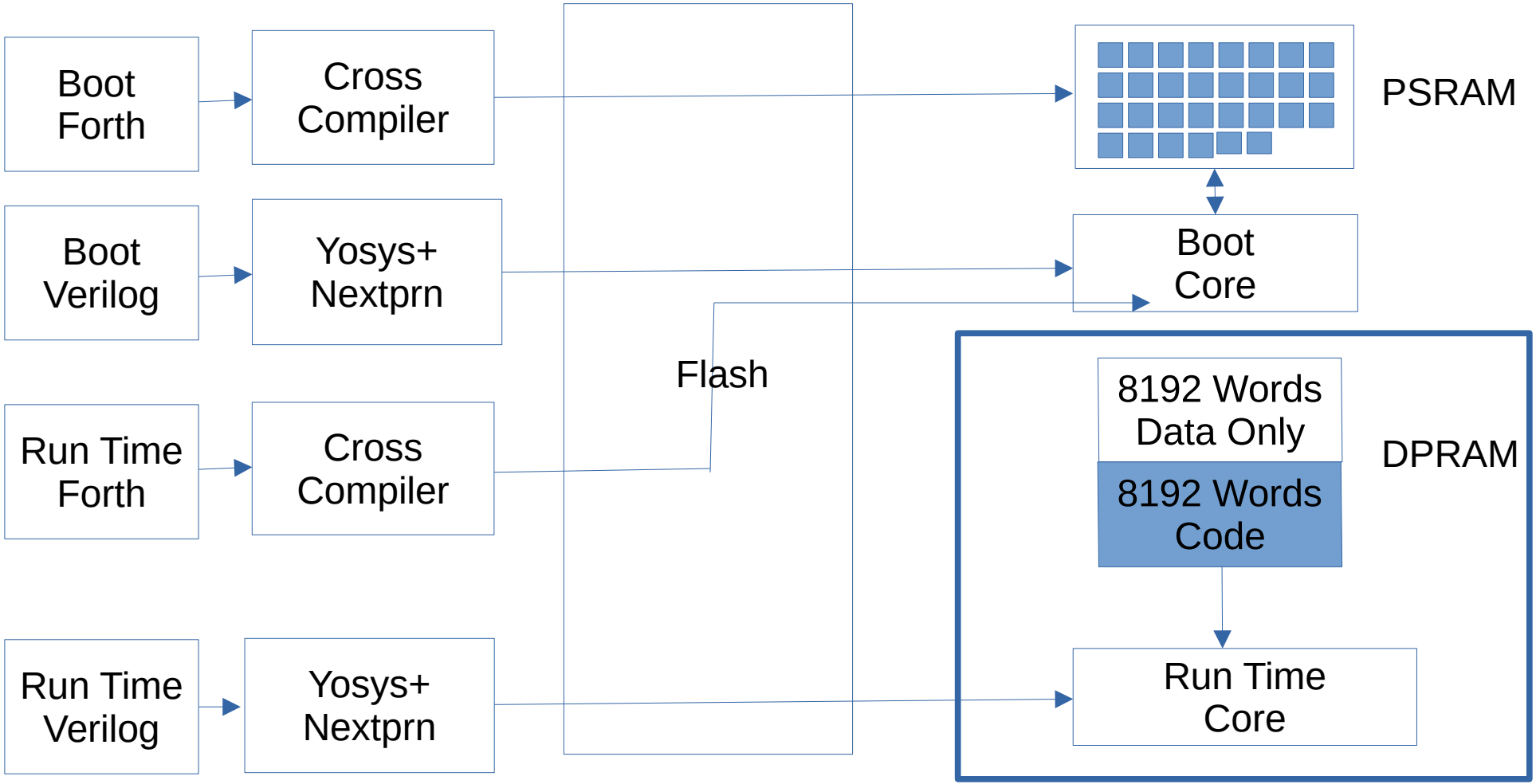
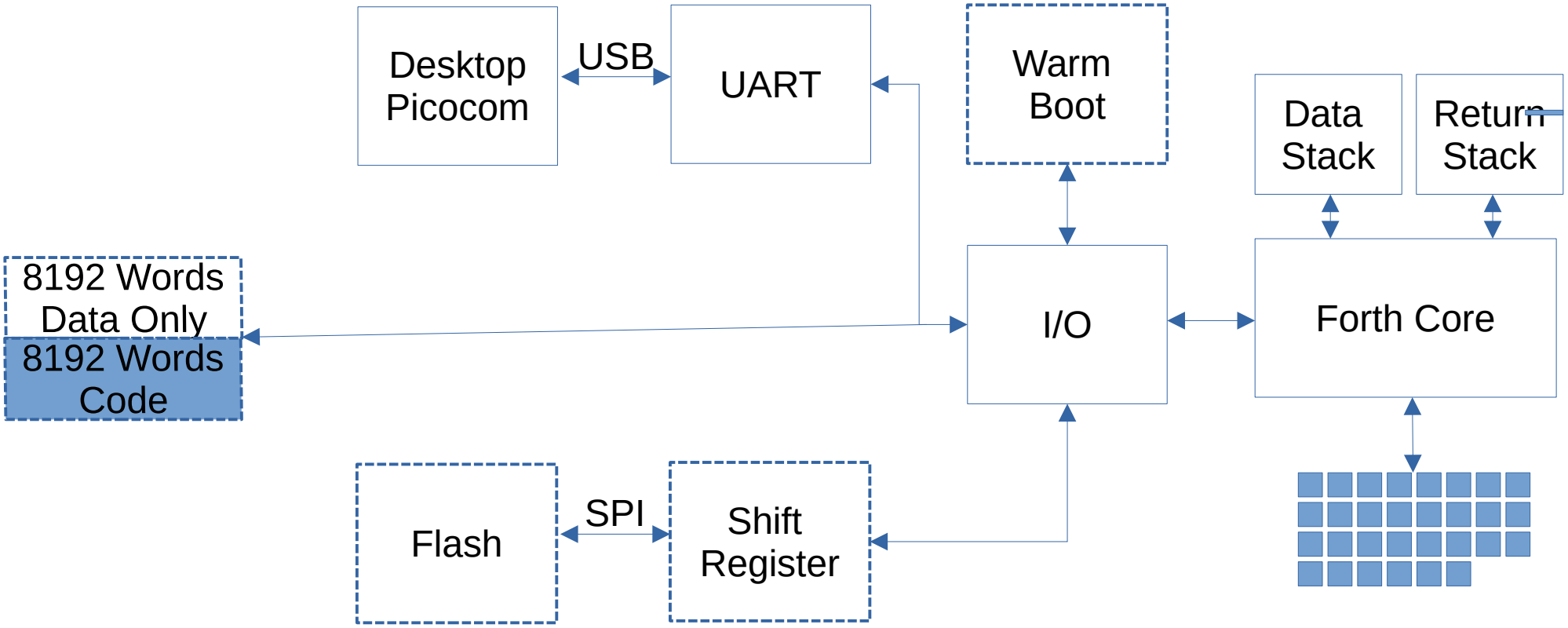
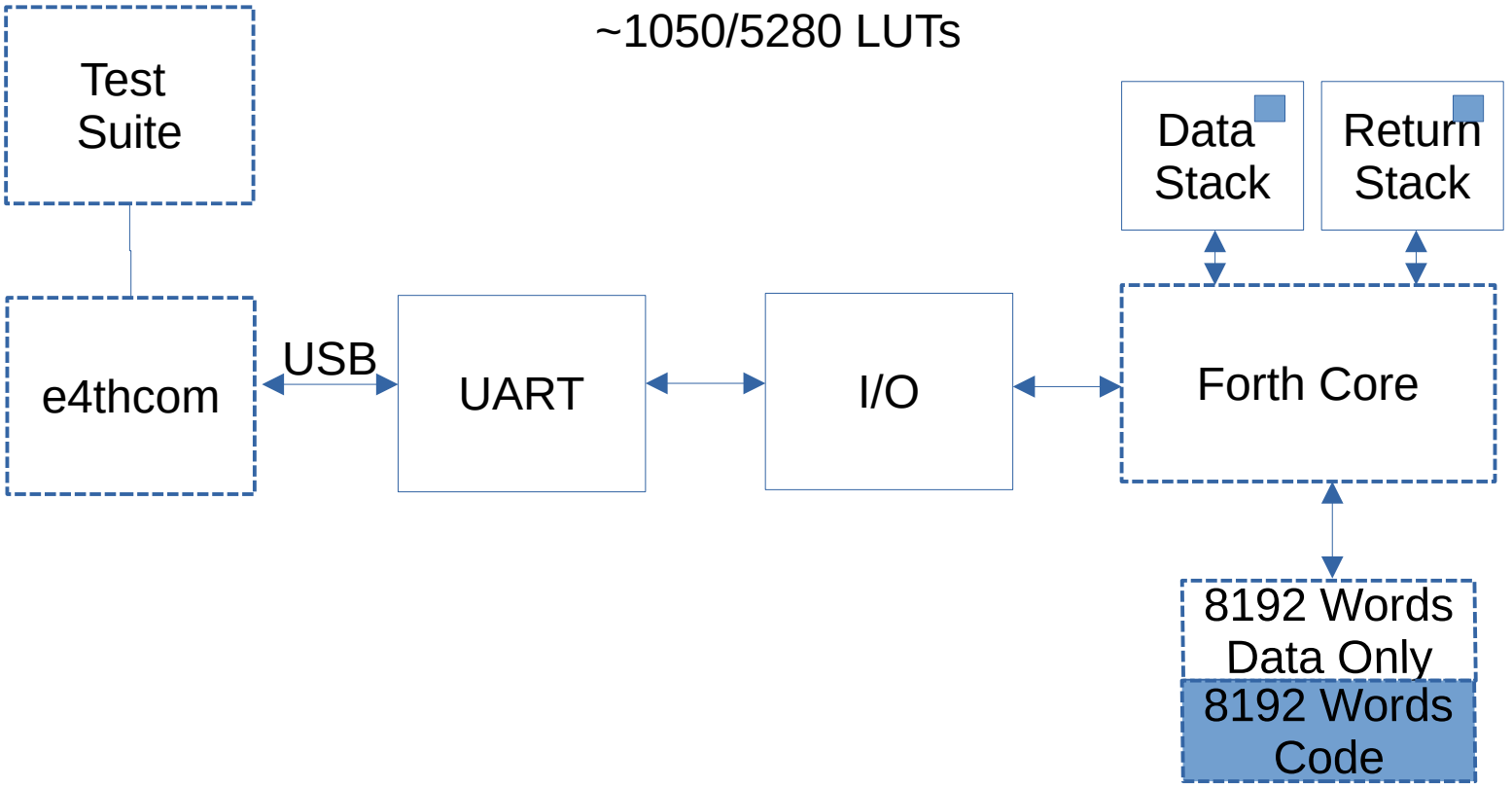


Boot Core


Desktop Picocom
USB
UART
Warm Boot
Data Stack
Return Stack
8192 Words Data Only
8192 Words Code
I/O
Forth Core
Flash
SPI
Shift Register

Run Time Core



e4thcom

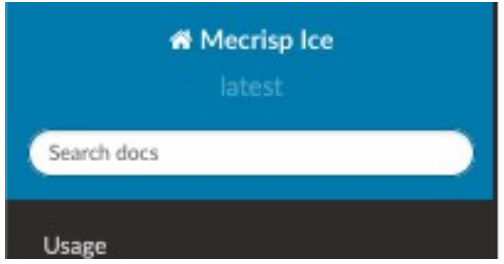
A Terminal for Embedded Forth Systems

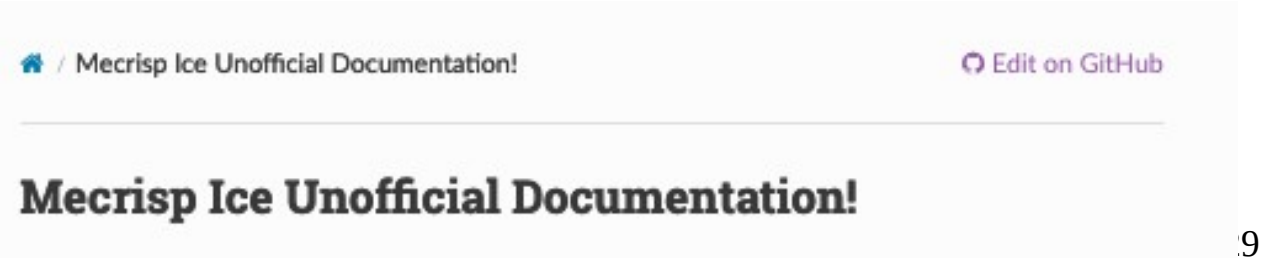
Supported Forth Systems:

328eForth , 430CamelForth , 430eForth , 4e4th, AmForth, anyForth , Mecrisp , Mecrisp-Quintus , Mecrisp-Stellaris , noForth , STM8 eForth , SwapForth

Status

Done	To Do
Reviewed Forth Soft Cores	Test Software
Reviewed J1 Family	15 bit data path
Shrank Mecrisp Ice	Boot Core
Single Port Forth and Verilog	SPI
Mecrisp Ice Documentation	Run Time Core
This Presentation	Finish Thesis
30 Pages Written	





Knowledge and Skills Acquired

Software	Hardware
OSS Cad Suite. APIO	Pico-Ice
Pico-Ice SDK	RP2040
Forth Cross Compiler	FLASH, HyperRAM
Eth4th	ICE40 SPI DSP Warm Boot
Hayes Forth Test Suite	

Questions?

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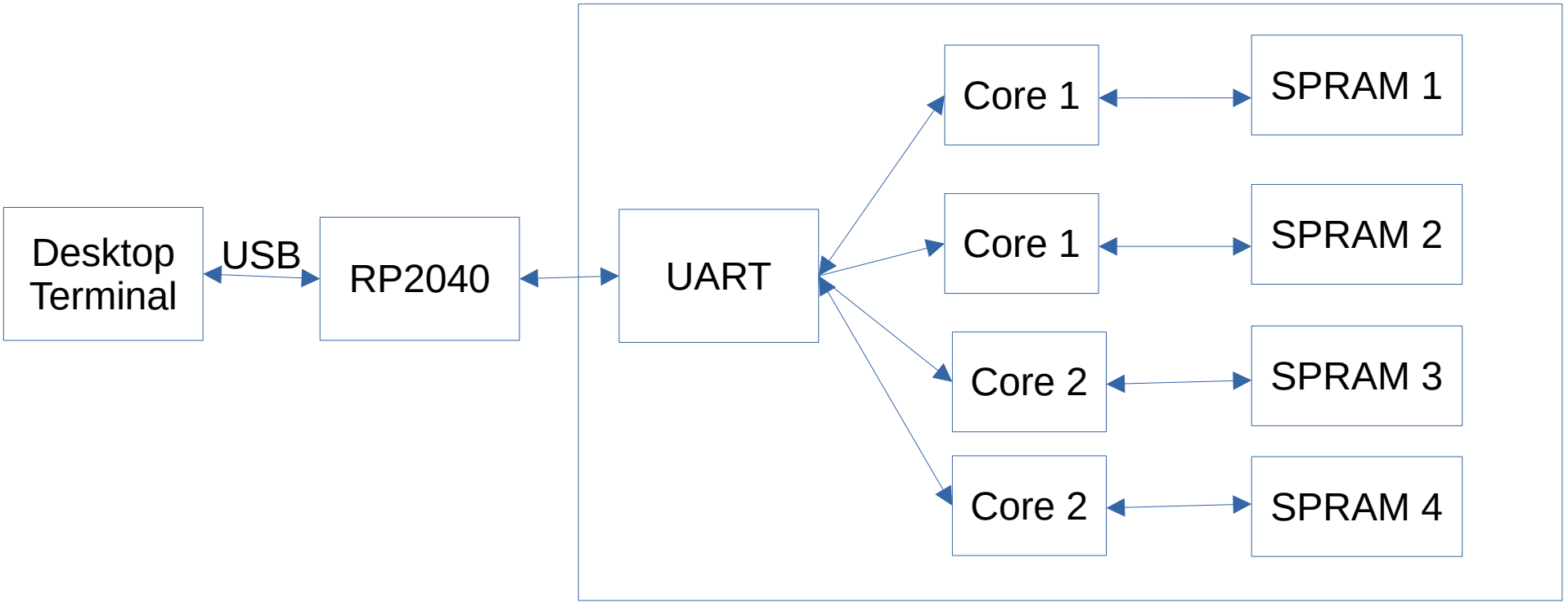
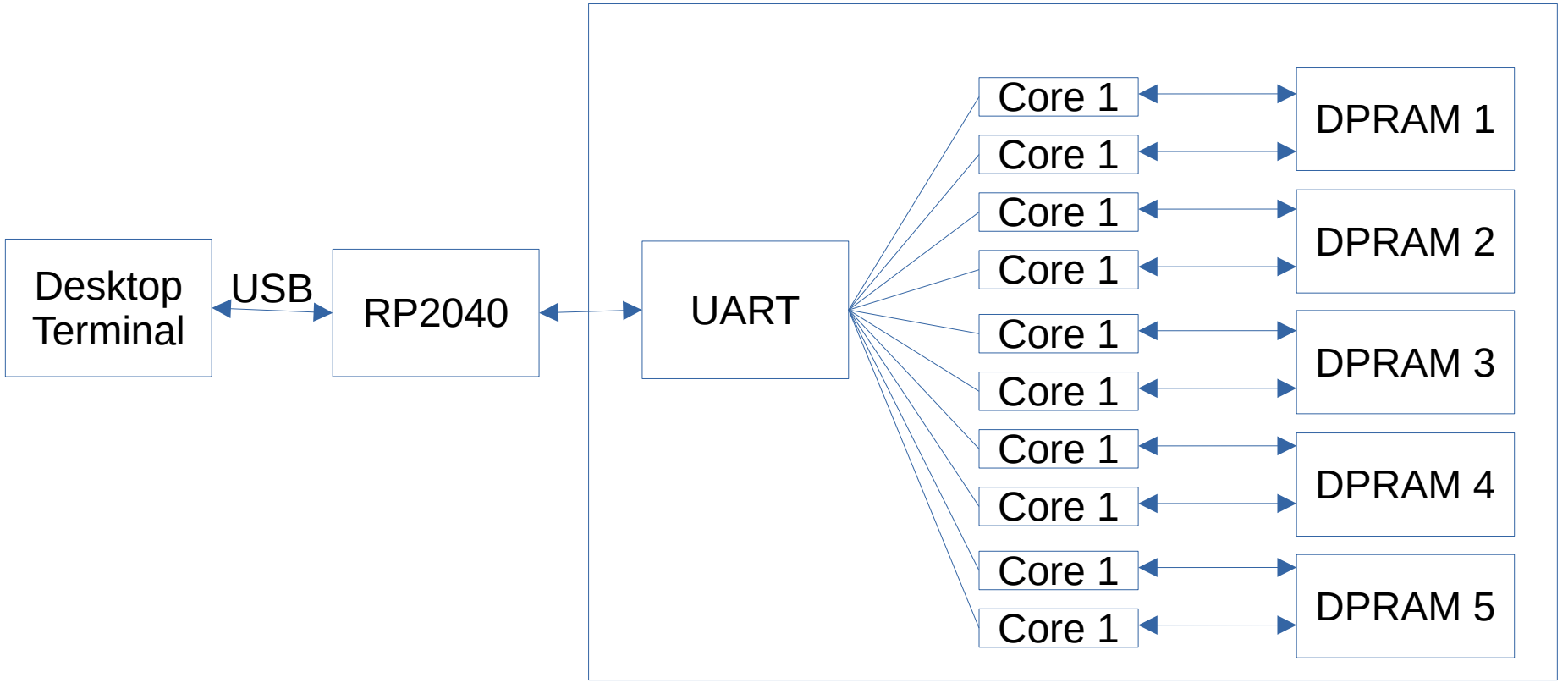
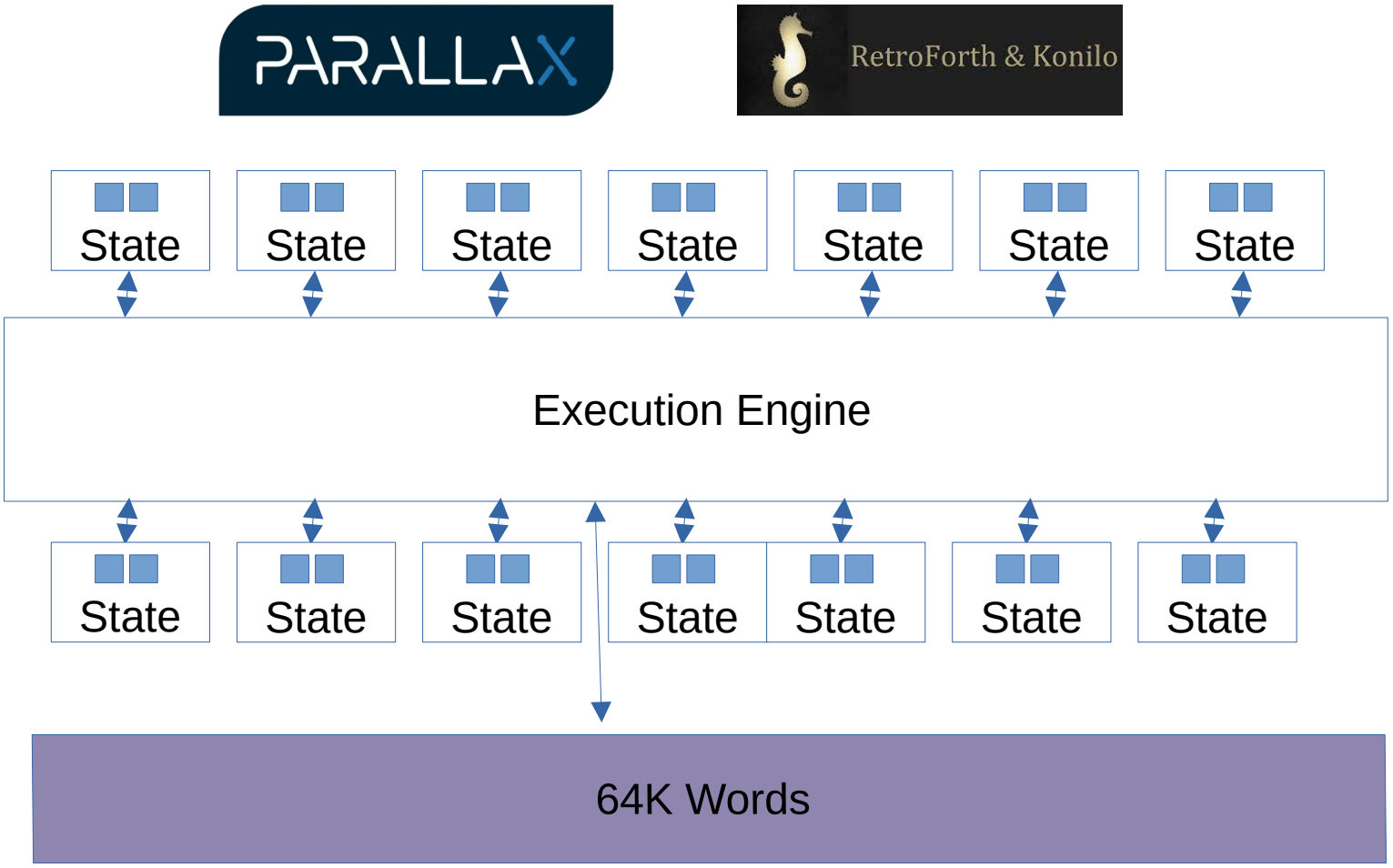
Future Work


Desktop Terminal
USB
RP2040
UART
Core 1
Core 1
Core 2
Core 2
SPRAM 1
SPRAM 2
SPRAM 3
SPRAM 4

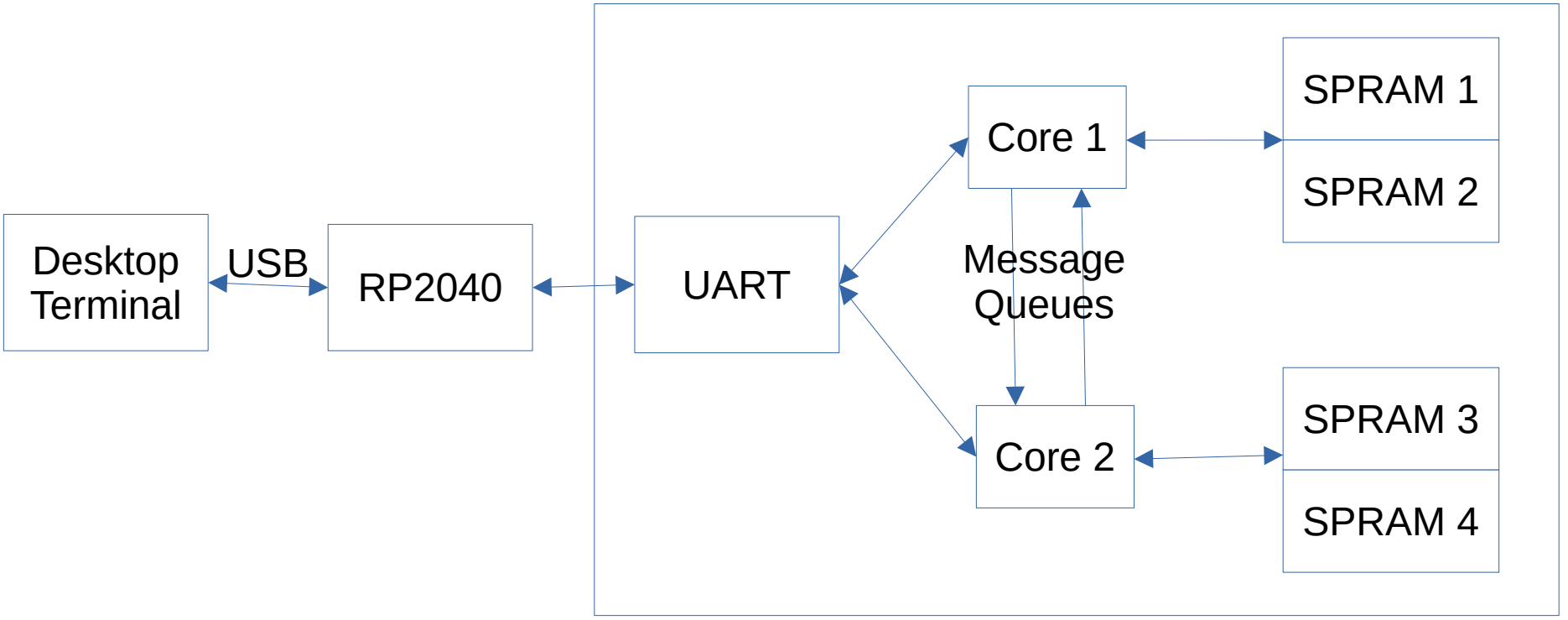
10 Cores on 5 DPRAMS



1-14 Barrel Processors



CSP Processor



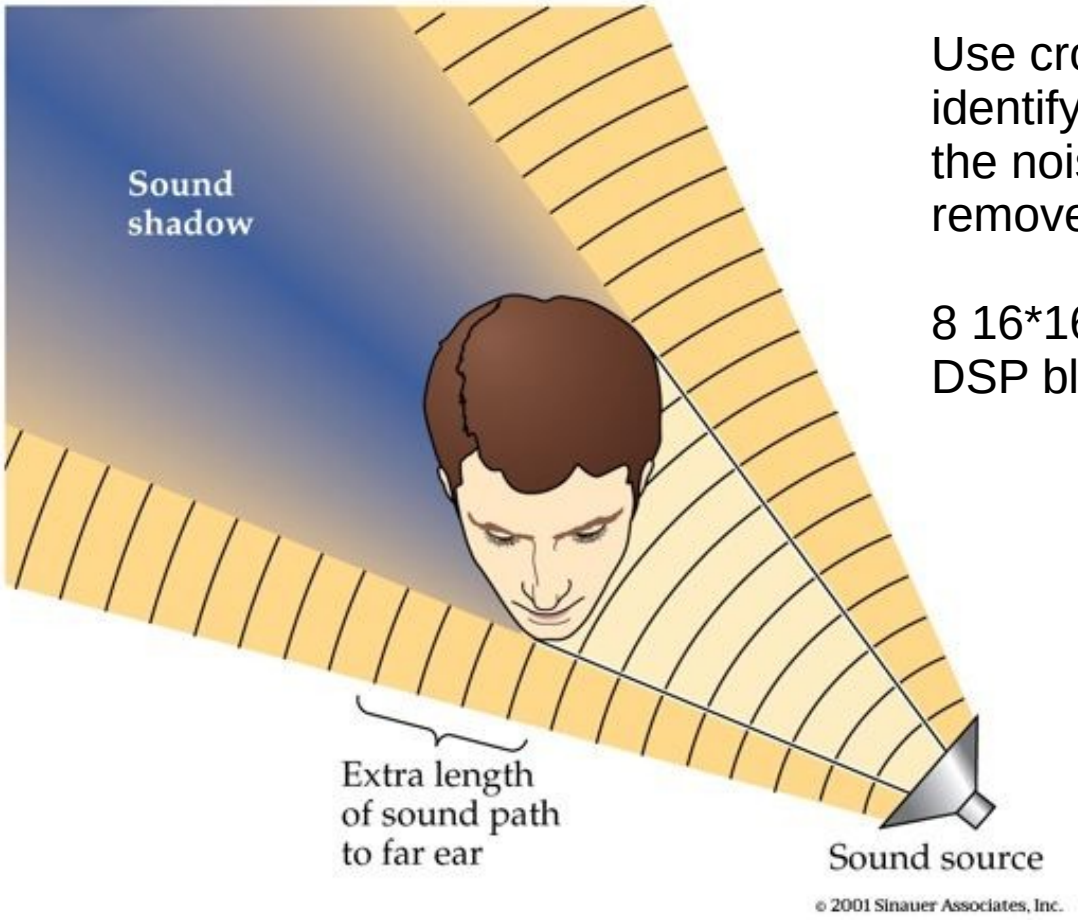
FishEye Undistort

Hearing Aids

Computational Audiology is considering adding an FPGA device.

Stereo Audio is 16 bits.
Ice 40 is a low power FPGA with 8*16 bit multipliers.
Many older Forthers need it.

Sound localization



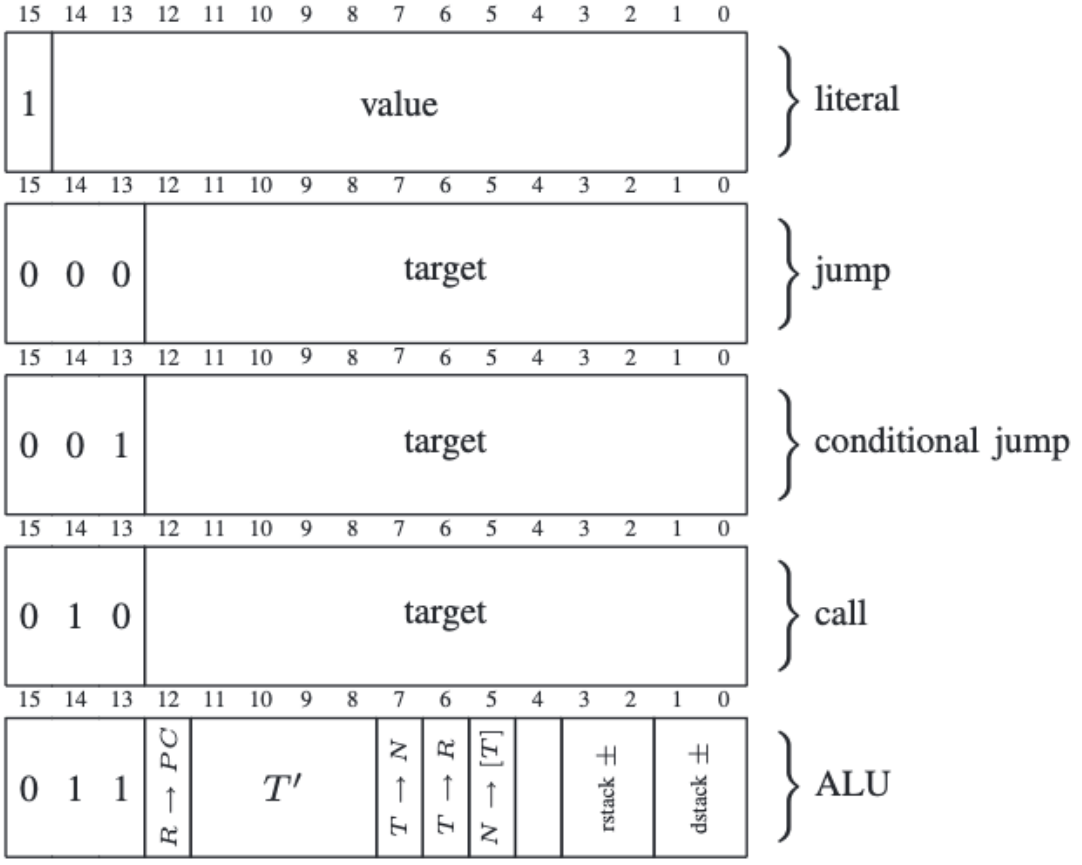
Use cross correlation to identify the angle of the noise sources and remove them.

8 16*16 multiply accumulate DSP blocks.

16 J1 Operations

0 T	8 N < T
1 N	9 N rshift T
2 T + N	10 T − 1
3 T and N	11 R
4 T or N	12 [T]
5 T xor N	13 N lshift T
6 ~ T	14 depth
7 N = T	15 N u<T

Instruction Format



Instruction CPU Flags

word	T'	$T \rightarrow N$	$R \rightarrow PC$	$T \rightarrow R$	dstack $\pm$	rstack $\pm$	$N \rightarrow [T]$
dup	T	•			+1	0	
over	N	•			+1	0	
invert	$\sim T$				0	0	
+	$T + N$				-1	0	
swap	N	•			0	0	
nip	T				-1	0	
drop	N				-1	0	
;	T		•		0	-1	
>r	N			•	-1	+1	
r>	R	•		•	+1	-1	
r@	R	•		•	+1	0	
@	$[T]$				0	0	
!	N				-1	0	•