Forth Day 2013

Evalboard Application
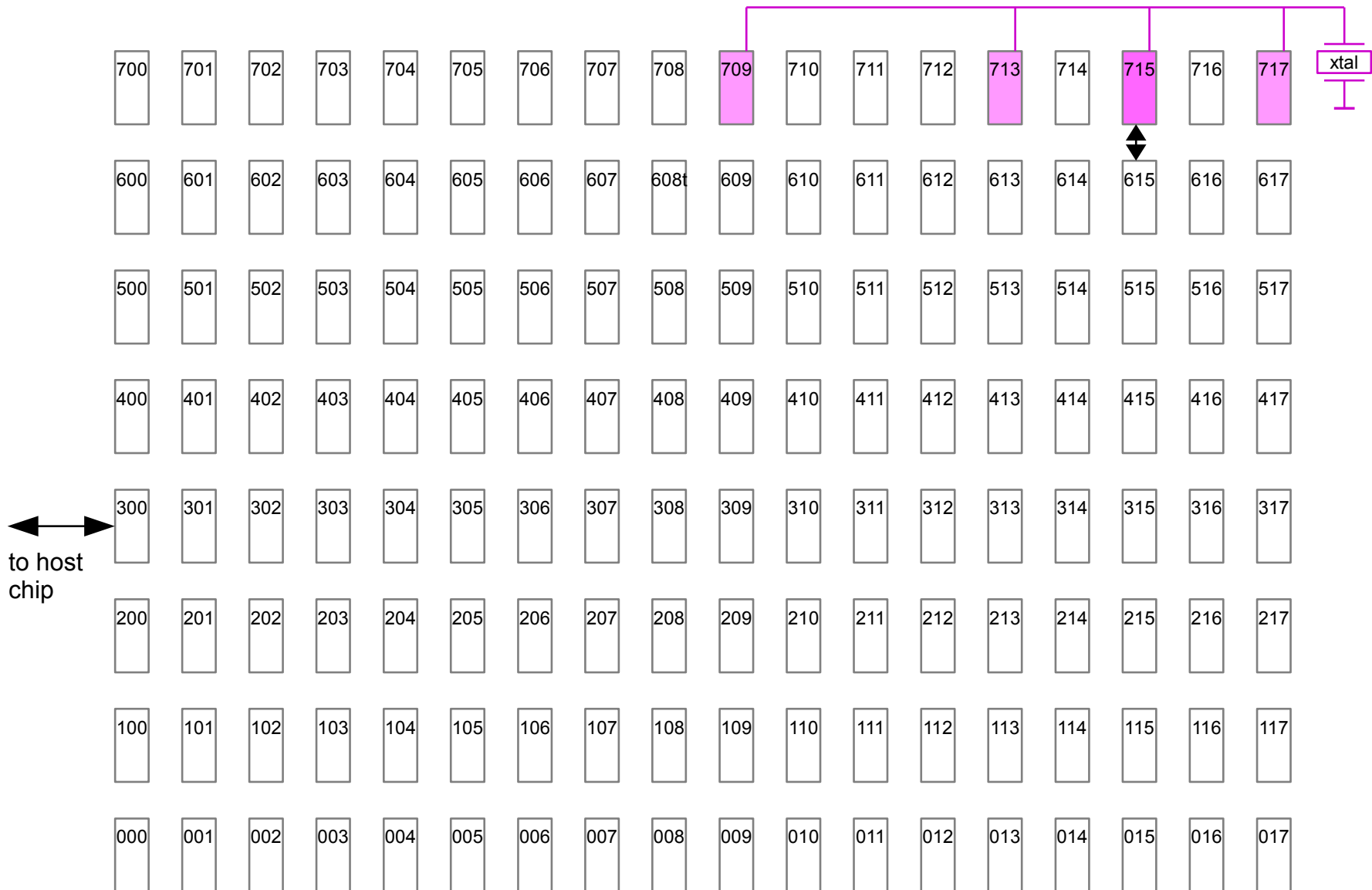
Low Frequency Clock
&
UART

Low Frequency Crystal Clock

- Only 1 Crystal @ 32'768 Hz needed

- Frequency search pattern

- Sustained clock operation

- Baud rate calibration
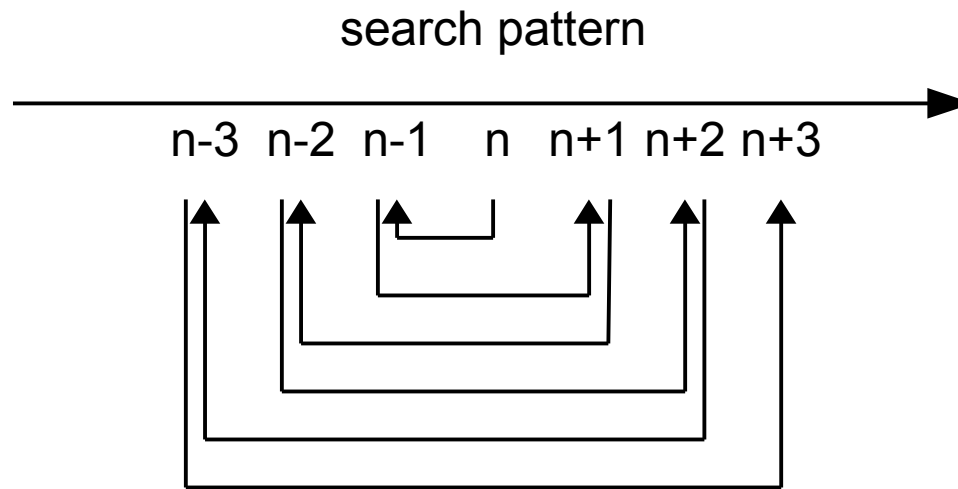
- Asynchronous communication

Clock Nodes

- The target chip (on the EVB001) is used

- Node 615 generates the search pattern

- Node 715 drives the crystal

- Node 717 picks up the clock signal

- F18 code from AN012 (sensortag)
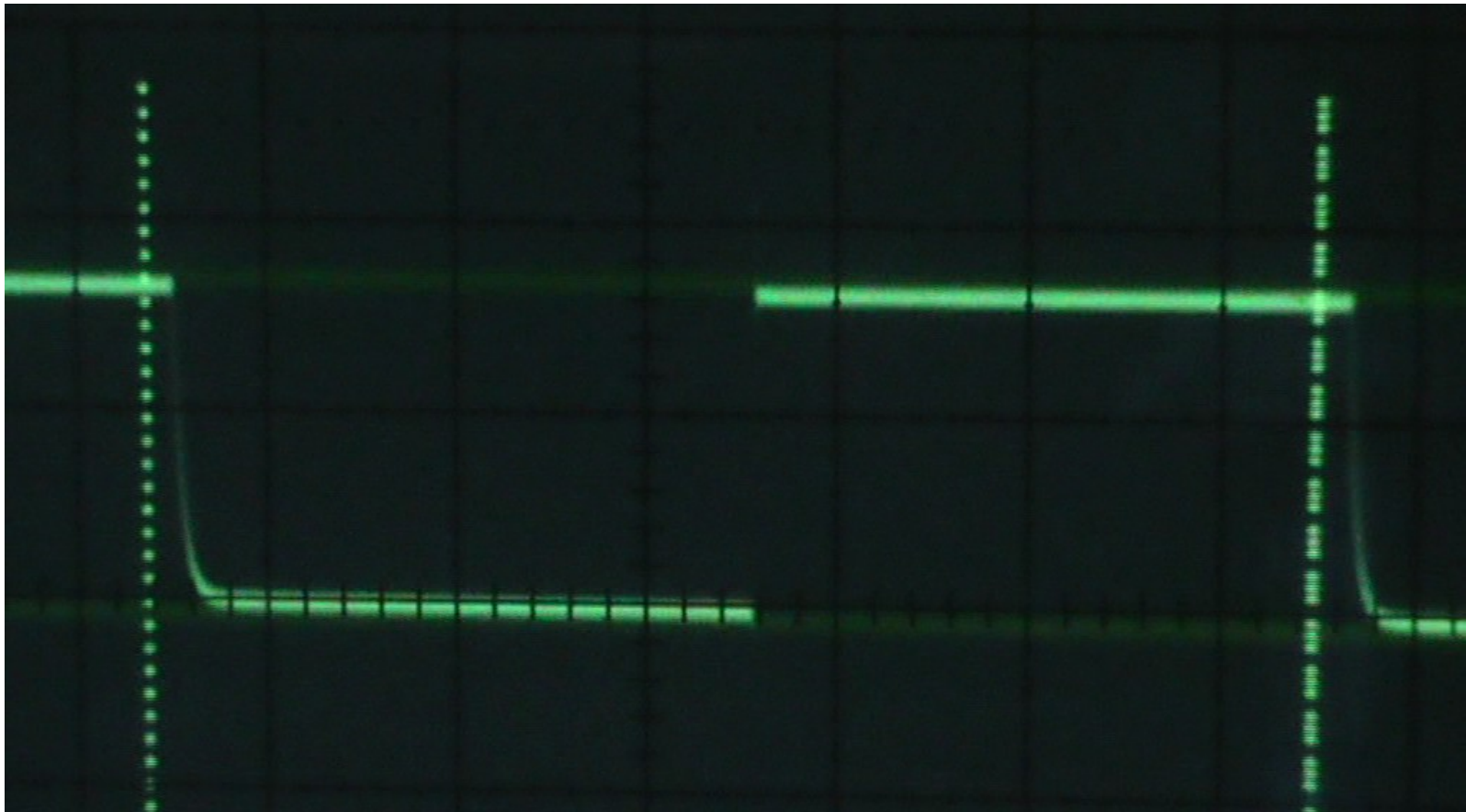
GA144 Node Allocation (clock)

700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	xtal
600	601	602	603	604	605	606	607	608t	609	610	611	612	613	614	615	616	617
500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517
400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417
300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317
200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217
100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117
000	001	002	003	004	005	006	007	008	009	010	011	012	013	014	015	016	017

to host
chip

Frequency Search Pattern

- Begin with an estimate

- Scan each side of the initial value until crystal frequency is matched
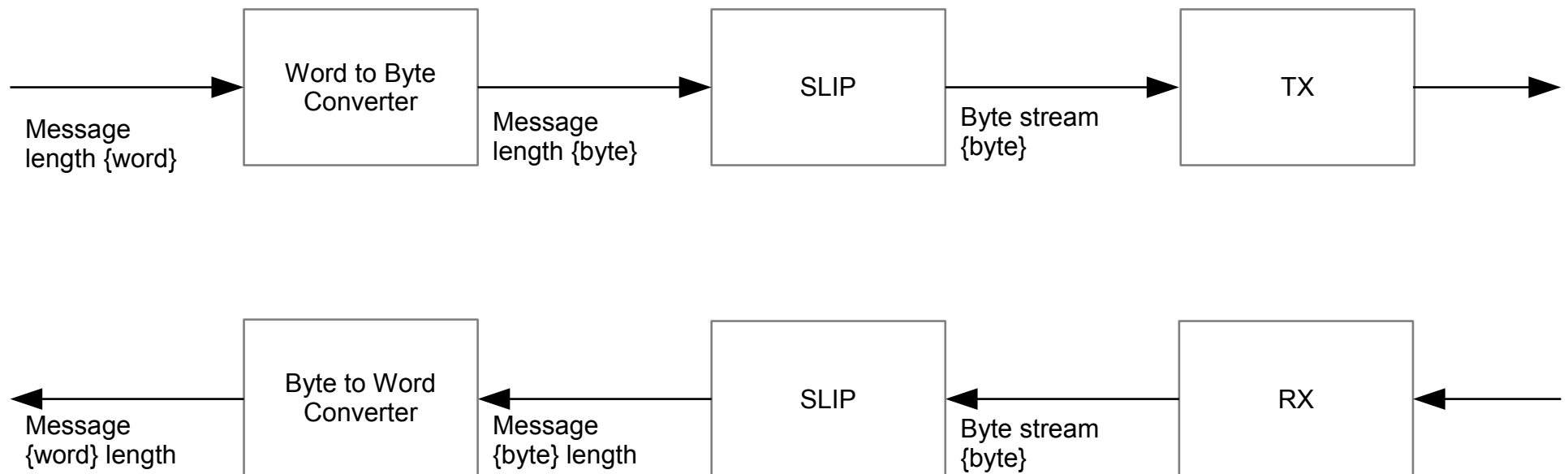
Clock Videos

UART

- Node 708 used for TX & CTS

- Node 517 used for RX

- Node 417 used for RTS

- Support for bluetooth host controller interface

Messaging

- Messages are used between host and bluetooth controller
- SLIP is used for message synchronisation

Timebase

- TX & RX nodes use 32 kHz clock for time calibration

- After measurements nodes 608 & 516 (dt) provide calculated looping values

Loop Measurement

```
-1 push
begin zif then <cond> until
pop -
```

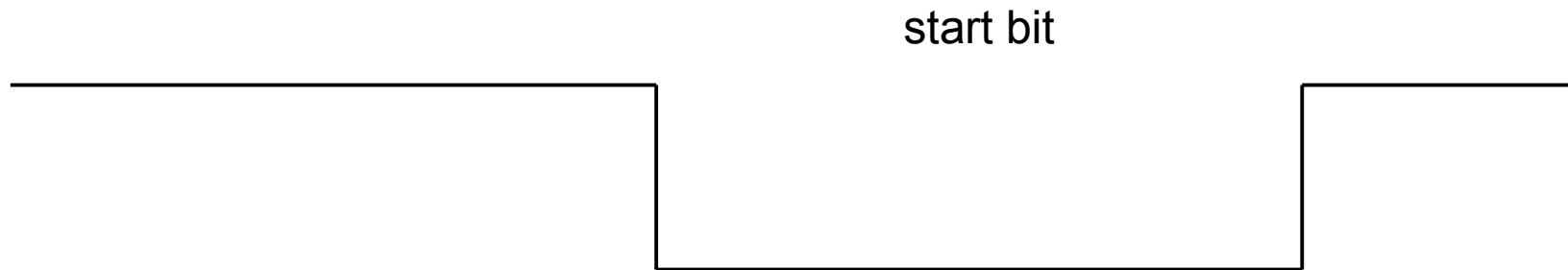- **zif then** decrements the index on the return stack

```
517 rx,
reclaim node 0 org b-io
wait1 00 dup dup or ahead
wait0 02 800 then 04 !b left a! @ drop ;
bitin nb 07 dup 2* push @b -if
high 09 drop or pop ; then drop drop pop ;
delay 0b right a! @ for unext ;
out 0f 2/ ff and down a! ! ;
calibrate n-m 13 push dup or - push up a!,
200 9 for dup unext,
1000 10 for @ drop unext,
begin drop @b and zif then until,
pop - pop . + 2/ ; 23 28 org
start 28 dup or !b,
dup or 7 for calibrate next
finish n- 2d right a! ! out
rx 30 wait1 wait0 dup or 1 delay,
8 for bitin delay delay next drop out rx ; 3d
```

1030

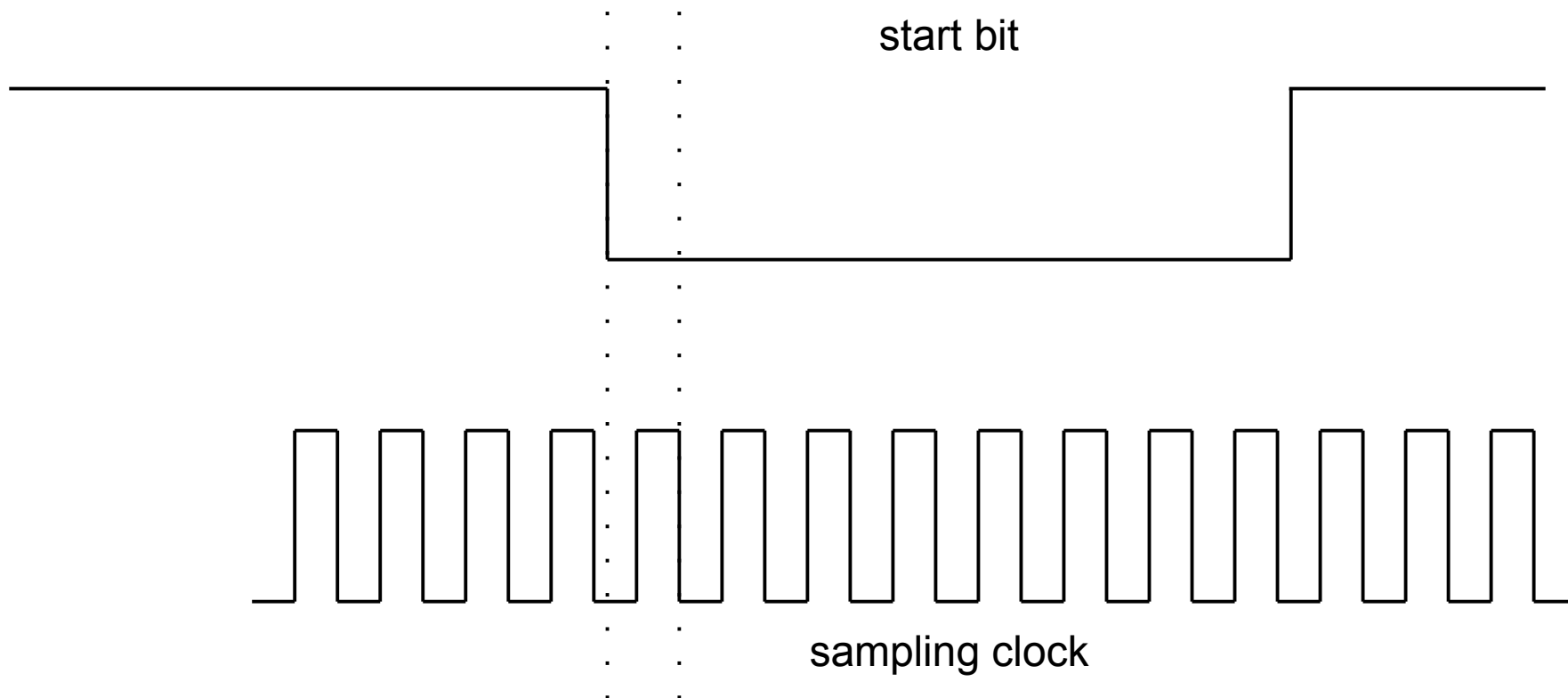w yrg*
cdfj ludr
edit ab k -mc+
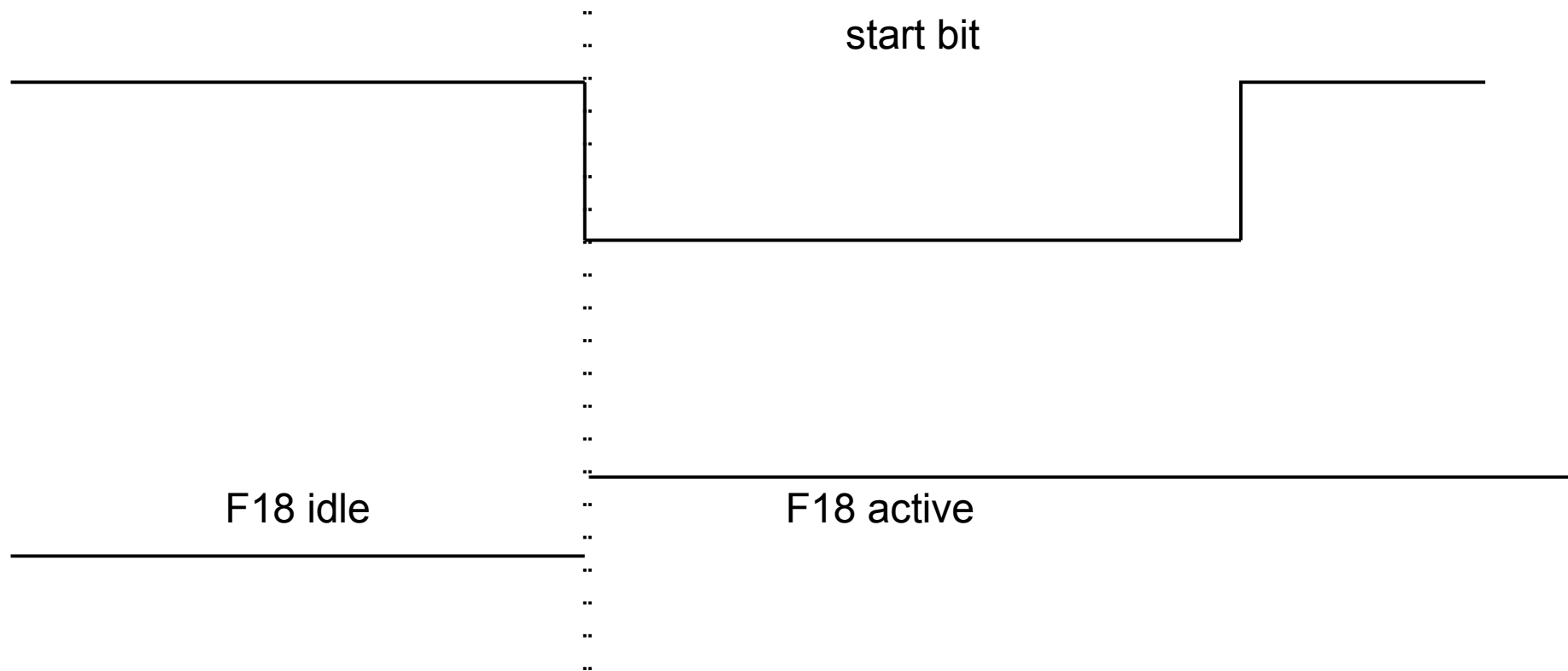x.i

Start Bit Timing

- Start bit can occur anytime

start bit

Conventional Start Bit Detection
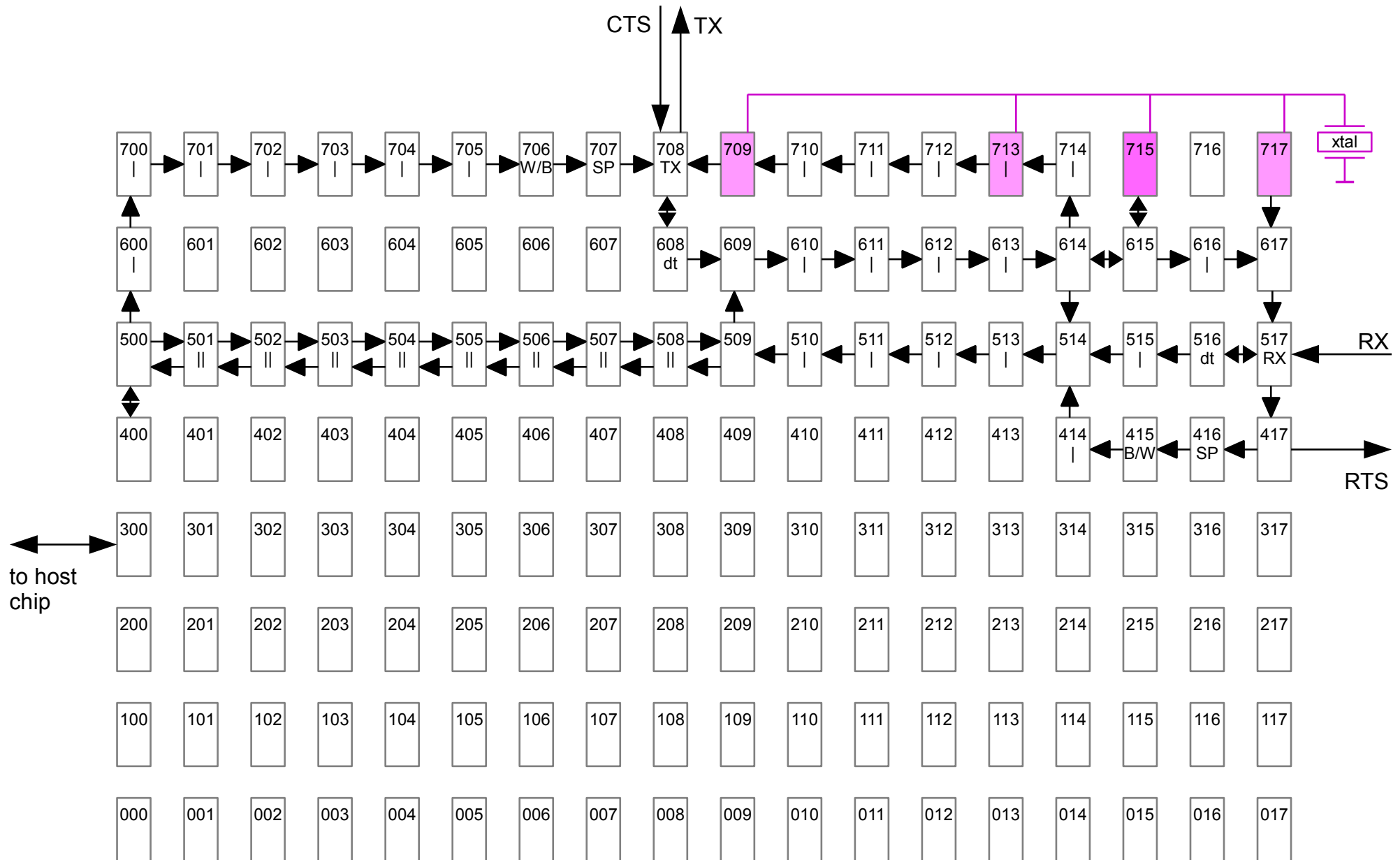
- Sampling frequency (16x baud rate)

start bit

sampling clock

F18 Start Bit Detection

- No sampling frequency
- Very low energy consumption when idle
- No sampling time error

start bit

F18 idle

F18 active

GA144 node allocation (UART test)

Video