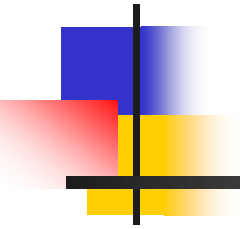
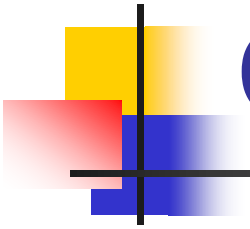


# A 32-Bit Computer for LatticeXP2 Brevia Development Kit

Silicon Valley FIG
December 18, 2010

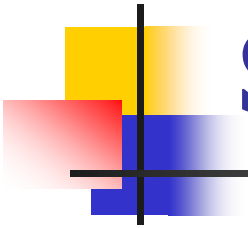
Chen-Hanson Ting



# Contents

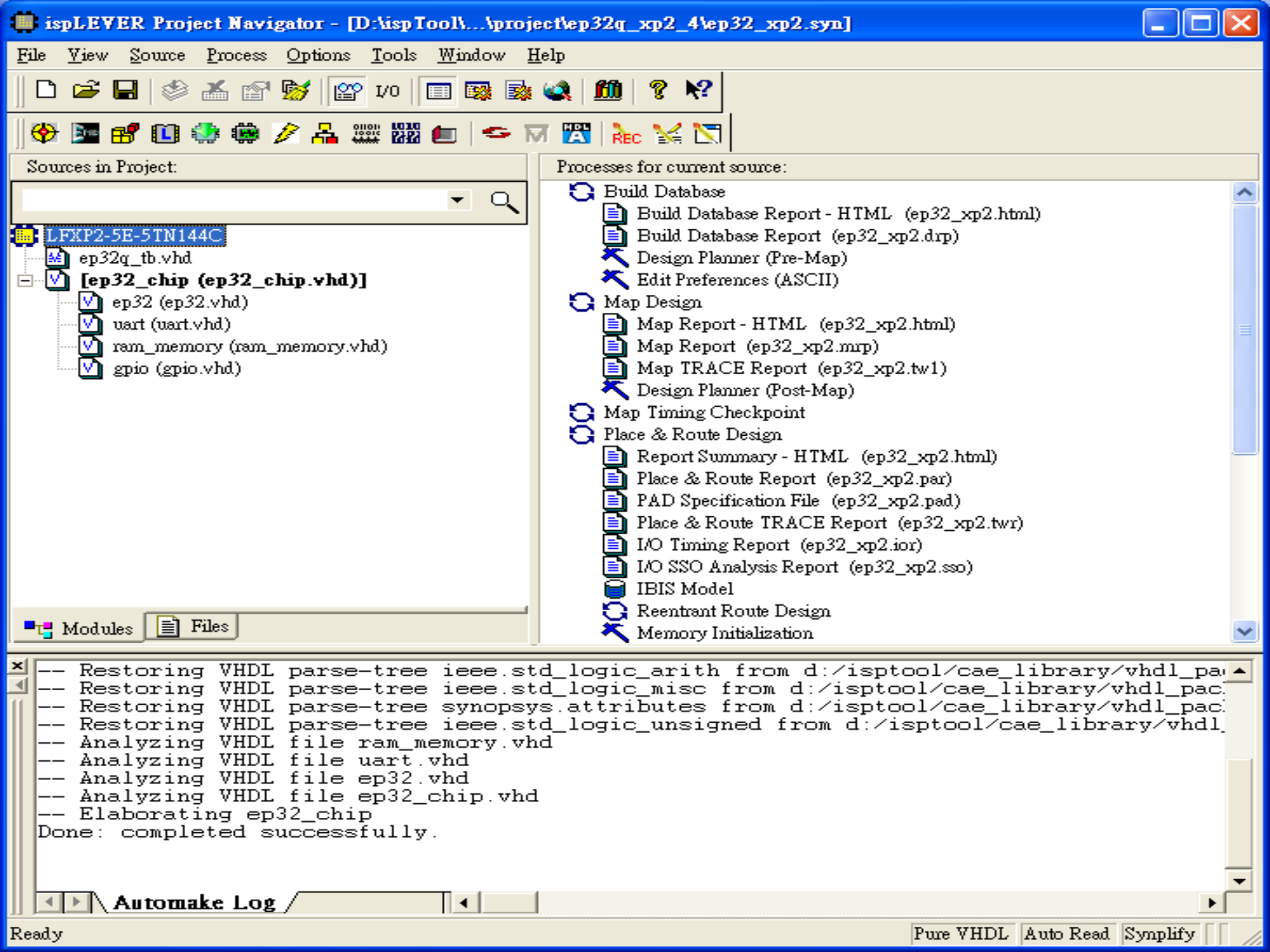
# Implement eP32 on Brevia Kit

- **Synthesis eP32**
- **Simulate eP32**
- **Layout eP32**
- **Download eP32**
- **Reveal eP32**



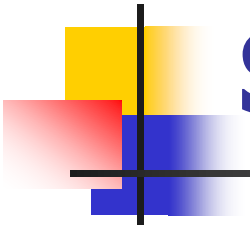
# Synthesis eP32

- Synplicity synthesis Tools
  - ep32_chip.vhd
  - ep32.vhd
  - ram_memory.vhd
  - uart.vhd
  - gpio.vhd


ispLEVER Project Navigator - [D:\ispTool\...\project\ep32q_xp2_4\ep32_xp2.syn]
File View Source Process Options Tools Window Help
I/O
Sources in Project:
LFXP2-5E-5TN144C
ep32q_tb.vhd
[ep32_chip (ep32_chip.vhd)]
ep32 (ep32.vhd)
uart (uart.vhd)
ram_memory (ram_memory.vhd)
gpio (gpio.vhd)
Modules
Files
Processes for current source:
Build Database
Build Database Report - HTML (ep32_xp2.html)
Build Database Report (ep32_xp2.drp)
Design Planner (Pre-Map)
Edit Preferences (ASCII)
Map Design
Map Report - HTML (ep32_xp2.html)
Map Report (ep32_xp2.mrp)
Map TRACE Report (ep32_xp2.tw1)
Design Planner (Post-Map)
Map Timing Checkpoint
Place & Route Design
Report Summary - HTML (ep32_xp2.html)
Place & Route Report (ep32_xp2.par)
PAD Specification File (ep32_xp2.pad)
Place & Route TRACE Report (ep32_xp2.twr)
I/O Timing Report (ep32_xp2.ior)
I/O SSO Analysis Report (ep32_xp2.sso)
IBIS Model
Reentrant Route Design
Memory Initialization
-- Restoring VHDL parse-tree ieee.std_logic_arith from d:/isptool/cae_library/vhdl_pa
-- Restoring VHDL parse-tree ieee.std_logic_misc from d:/isptool/cae_library/vhdl_pac
-- Restoring VHDL parse-tree synopsys.attributes from d:/isptool/cae_library/vhdl_pac
-- Restoring VHDL parse-tree ieee.std_logic_unsigned from d:/isptool/cae_library/vhdl
-- Analyzing VHDL file ram_memory.vhd
-- Analyzing VHDL file uart.vhd
-- Analyzing VHDL file ep32.vhd
-- Analyzing VHDL file ep32_chip.vhd
-- Elaborating ep32_chip
Done: completed successfully.
Automake Log
Ready
Pure VHDL
Auto Read
Symplify

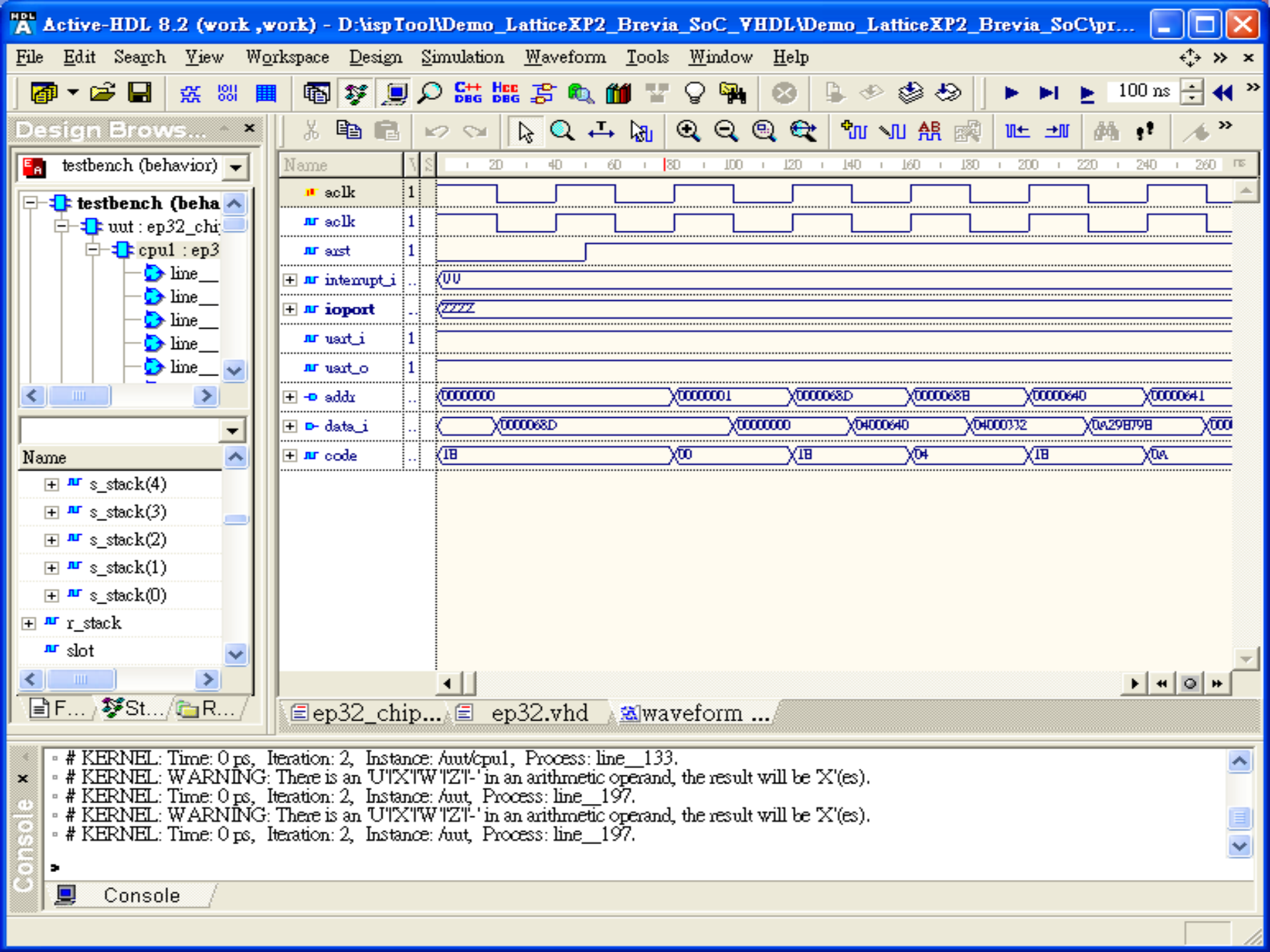
# Synthesis eP32

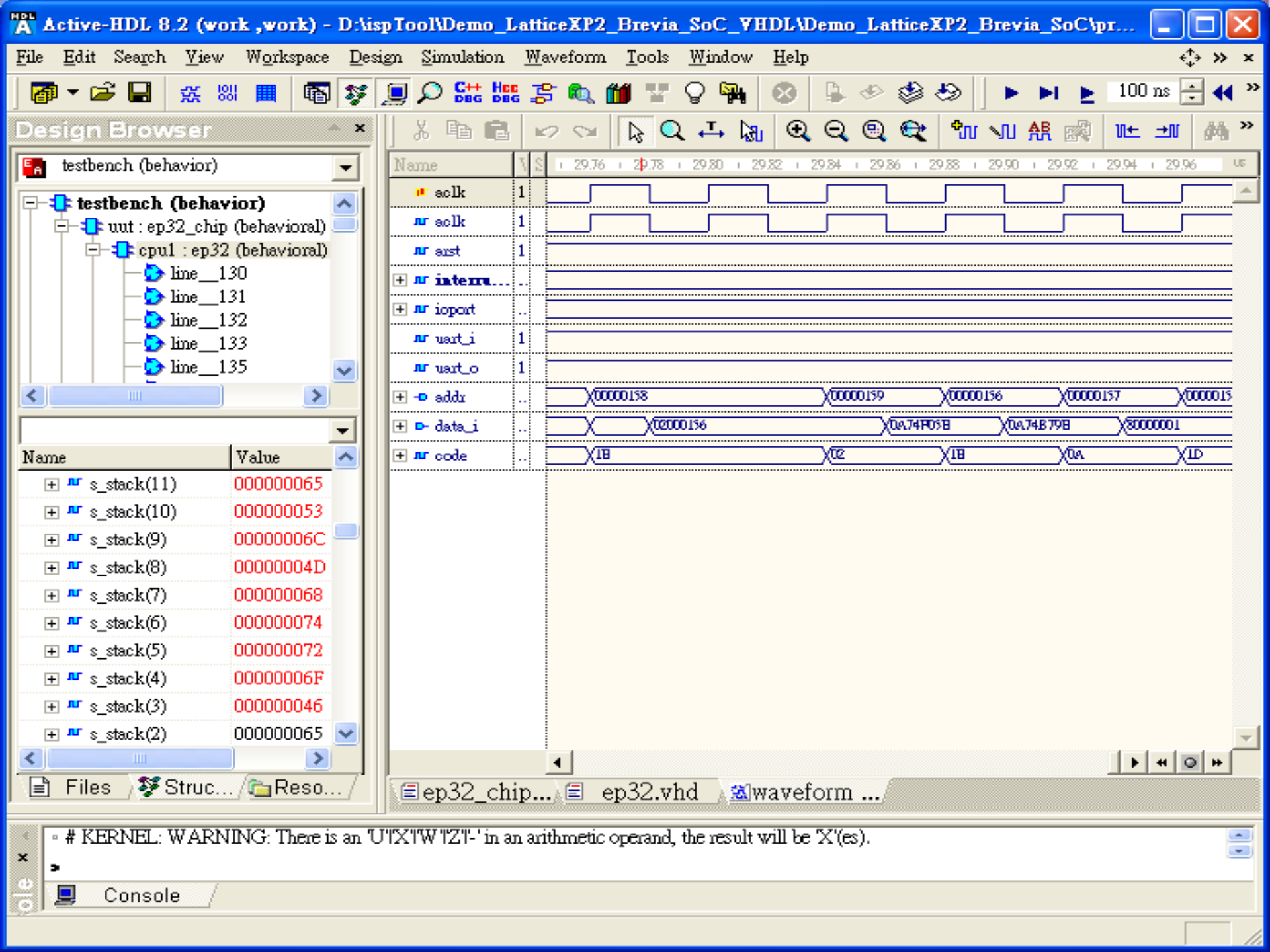
- Only ram_memory.vhd must be reconstructed to use RAM_Q modules in LatticeXP2-5E FPGA chip.
- Ep32q.mem is produced by eForth metacompiler to initialize RAM_Q modules in XP2.



# Simulate eP32

- Active-HDL simulation tools supplied by Aldec
- Need a test bench module to test eP32 chip.
- Activate ep32q_tb.vhd for functional simulation


Active-HDL 8.2 (work ,work) - D:\ispTool\Demo_LatticeXP2_Brevia_SoC_VHDL\Demo_LatticeXP2_Brevia_SoC\pr...
File Edit Search View Workspace Design Simulation Waveform Tools Window Help
100 ns
Design Brows...
testbench (behavior)
testbench (beha
uut : ep32_chi
cpu1 : ep3
line__
line__
line__
line__
line__
Name
s_stack(4)
s_stack(3)
s_stack(2)
s_stack(1)
s_stack(0)
r_stack
slot
F...
St...
R...
Name
aclk
aclk
arst
interrupt_i
ioport
uart_i
uart_o
addr
data_i
code
20 40 60 80 100 120 140 160 180 200 220 240 260
UU
ZZZZ
00000000 00000001 0000068D 0000068B 00000640 00000641
0000068D 00000000 04000640 04000332 0a29B79B
1B 00 1B 04 1B 0A
ep32_chip...
ep32.vhd
waveform ...
# KERNEL: Time: 0 ps, Iteration: 2, Instance: /uut/cpu1, Process: line__133.
# KERNEL: WARNING: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
# KERNEL: Time: 0 ps, Iteration: 2, Instance: /uut, Process: line__197.
# KERNEL: WARNING: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
# KERNEL: Time: 0 ps, Iteration: 2, Instance: /uut, Process: line__197.
Console
Console

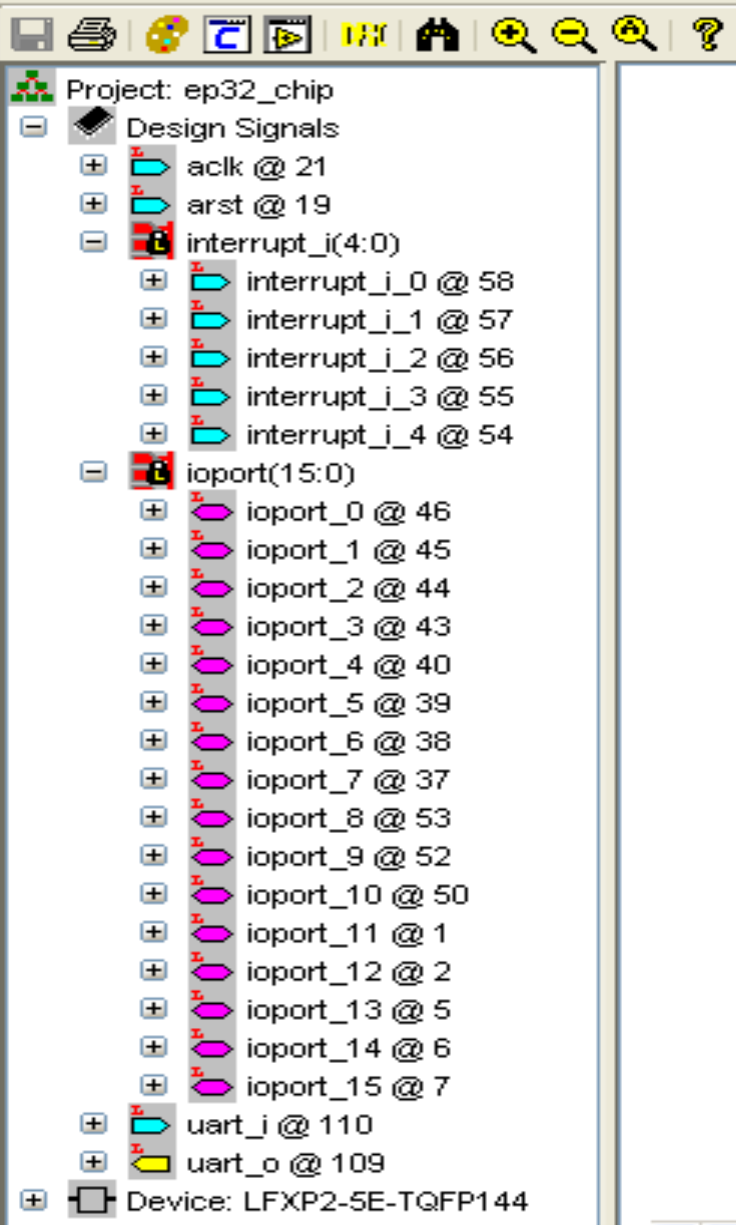

Active-HDL 8.2 (work ,work) - D:\ispTool\Demo_LatticeXP2_Brevia_SoC_VHDL\Demo_LatticeXP2_Brevia_SoC\pr...
File Edit Search View Workspace Design Simulation Waveform Tools Window Help
100 ns
Design Browser
testbench (behavior)
testbench (behavior)
uut : ep32_chip (behavioral)
cpu1 : ep32 (behavioral)
line__130
line__131
line__132
line__133
line__135
Name
Value
s_stack(11) 00000065
s_stack(10) 00000053
s_stack(9) 0000006C
s_stack(8) 0000004D
s_stack(7) 00000068
s_stack(6) 00000074
s_stack(5) 00000072
s_stack(4) 0000006F
s_stack(3) 00000046
s_stack(2) 00000065
Files
Struc...
Reso...
Name
29.76
29.78
29.80
29.82
29.84
29.86
29.88
29.90
29.92
29.94
29.96
us
aclk 1
aclk 1
arst 1
interru... ..
ioport ..
uart_i 1
uart_o 1
addr ..
00000158
00000159
00000156
00000157
data_i ..
02000156
0A74F058
0A74B798
80000001
code ..
1B
02
1B
0A
1D
ep32_chip...
ep32.vhd
waveform ...
# KERNEL: WARNING: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
Console

# Layout eP32

- Invoke Design Planner to connect following signals
  - External reset
  - External master clock
  - Interrupts
  - GPIO to LED and switches
  - UART transmit
  - UART receiver

Package View (ep32_xp2.lpf)

File Edit View Tools Help

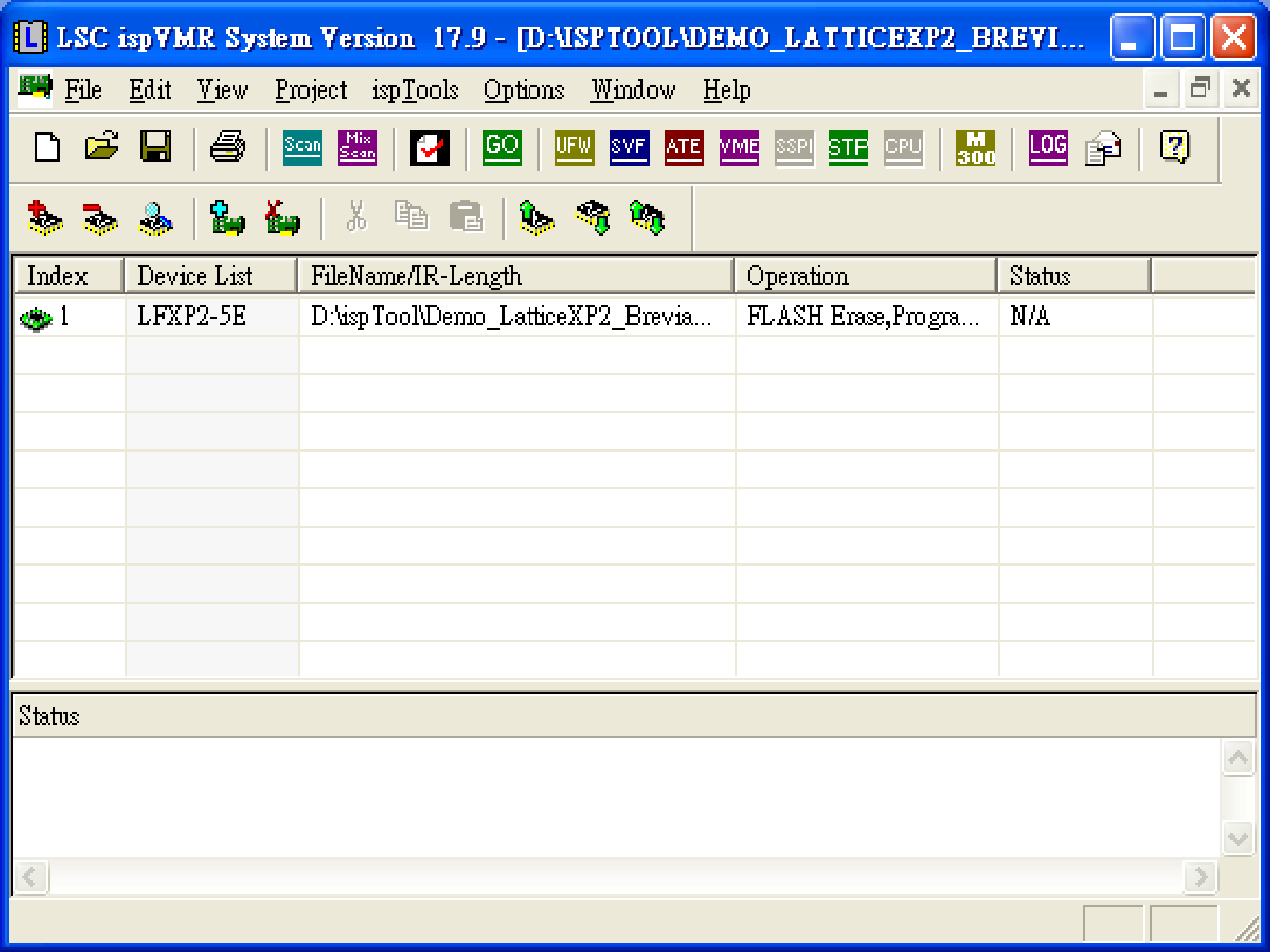




Site 60:VCCAUX; Bank 99: 0 assigned/27 total

# Download eP32

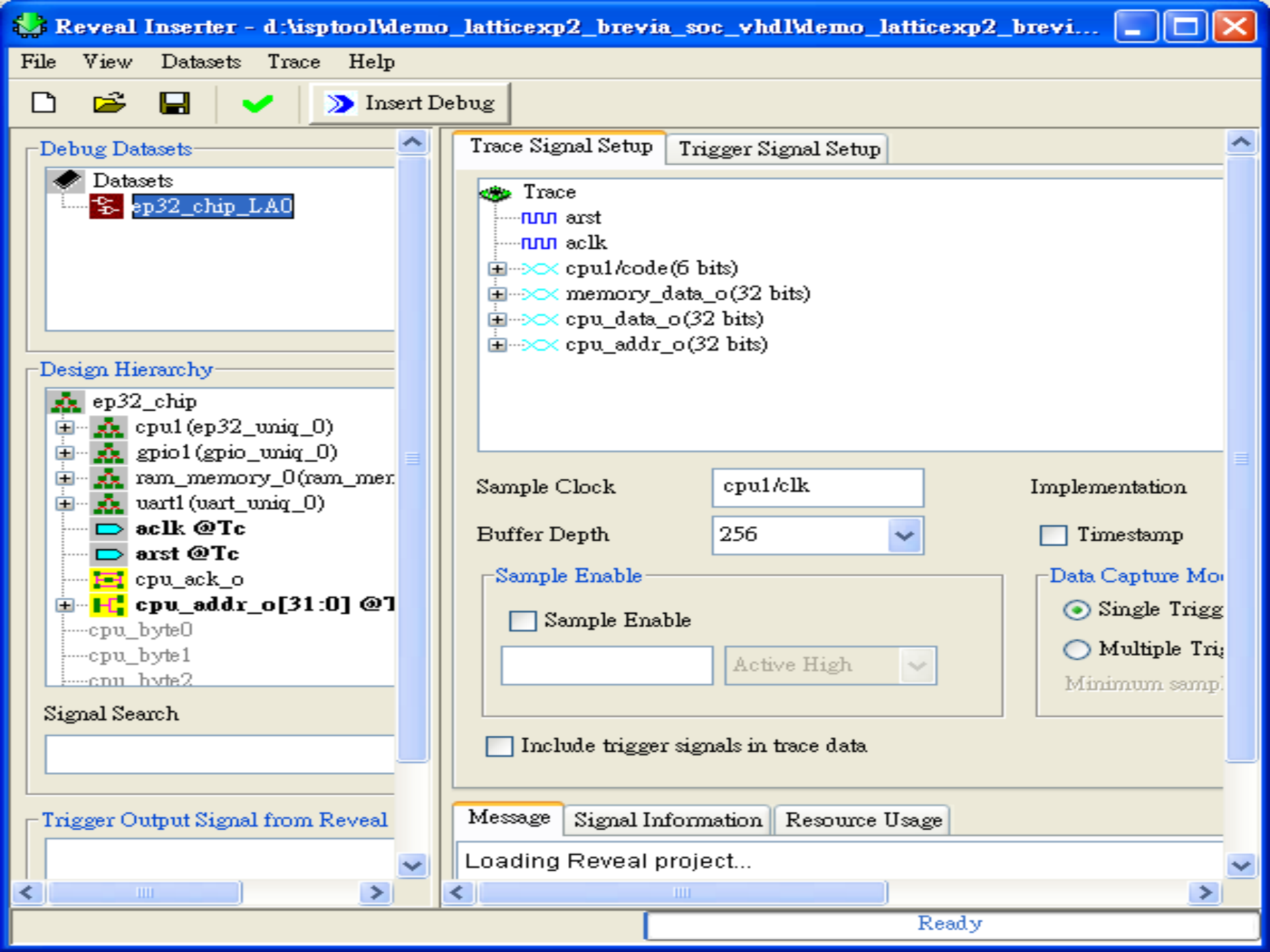
- JTAP cable connected to printer port
- UART cable connected to COM port
- Invoke ispVM system to download ep32_xp2.jed file
- eP32 eForth signs on Hyperterminal

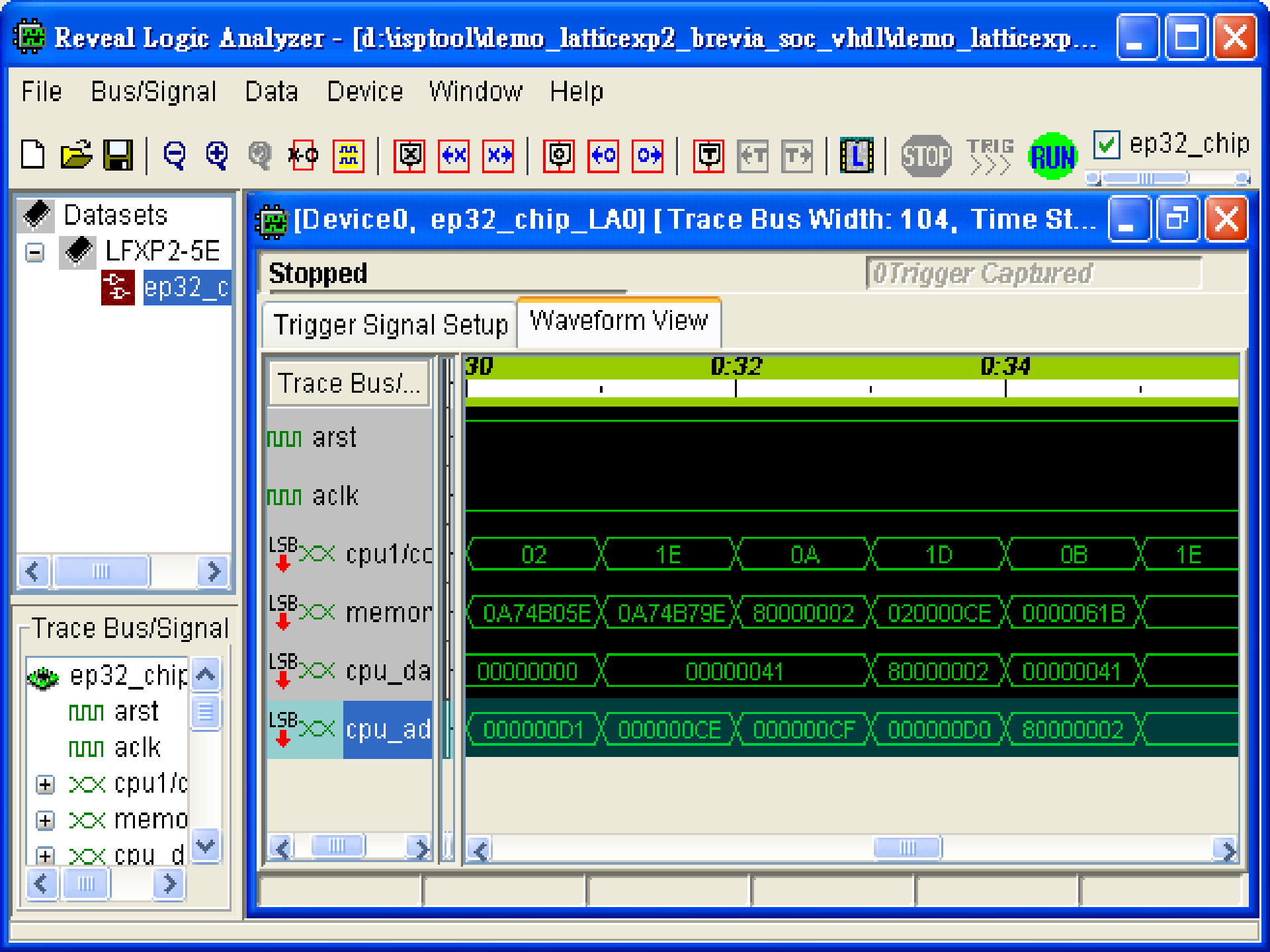

LSC ispVMR System Version 17.9 - [D:\ISPTOOL\DEMO_LATTICEXP2_BREVI...
File Edit View Project ispTools Options Window Help
Scan
Mix Scan
GO
UFW
SVF
ATE
VME
SSPI
STP
CPU
M 300
LOG
Index
Device List
FileName/IR-Length
Operation
Status
1
LFXP2-5E
D:\ispTool\Demo_LatticeXP2_Brevia...
FLASH Erase,Progra...
N/A
Status

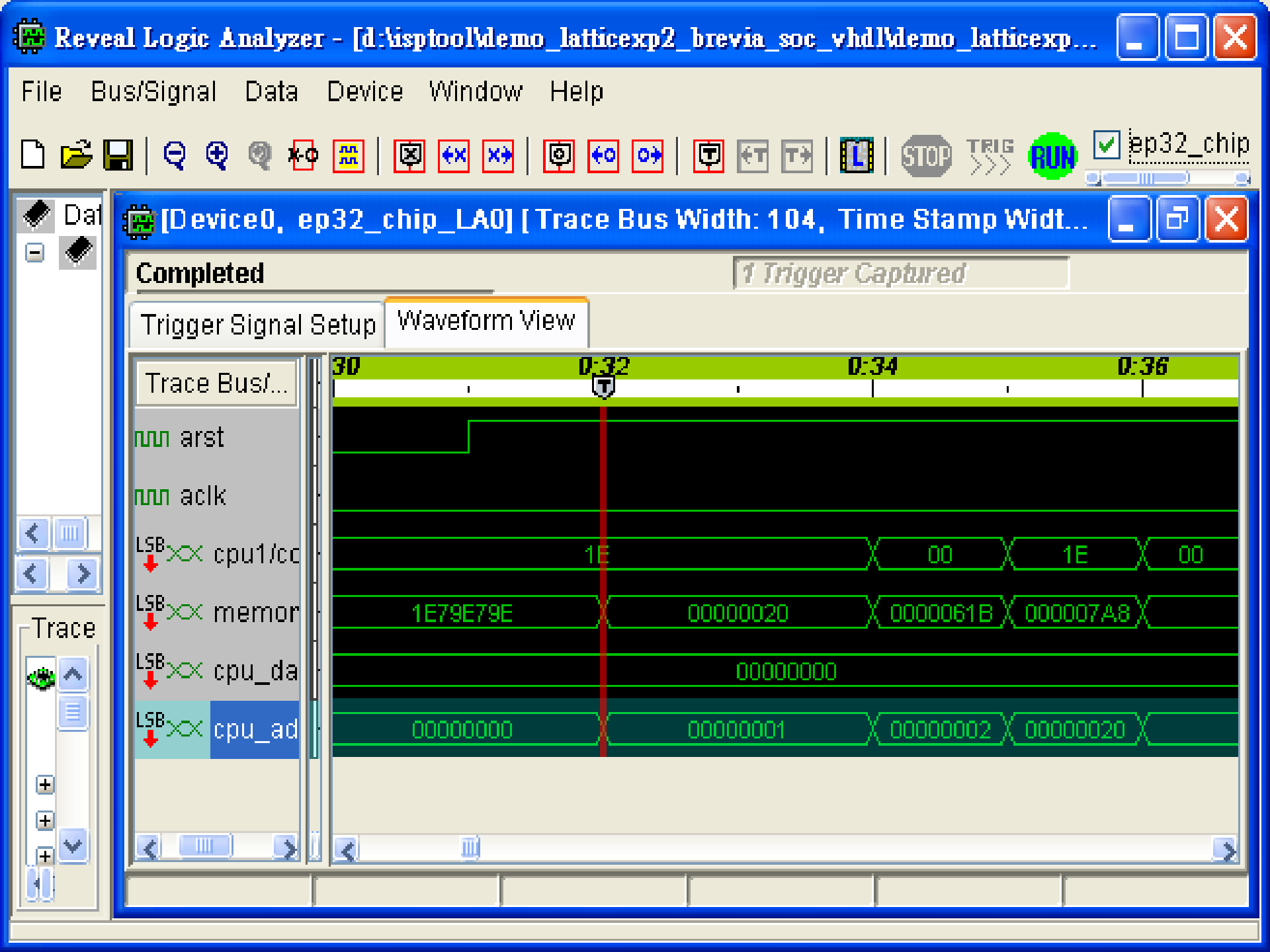

115200 - 超級終端機
檔案(F) 編輯(E) 檢視(V) 呼叫(C) 轉送(T) 說明(H)
OK
OK
eP32q v2.05

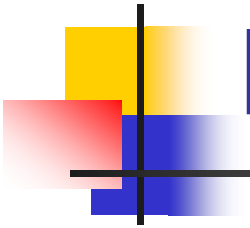
# Reveal eP32

- Invoke Reveal Inserter to insert debugging logic and tracing memory
- Invoke Synplicity to synthesize modified chip design
- Download tp XP2 chip with ispVM
- Invoke Reveal Logic Analyzer to trace selected internal signals


Reveal Inserter - d:\isptool\demo_latticexp2_brevia_soc_vhdl\demo_latticexp2_brevi...
File
View
Datasets
Trace
Help
Insert Debug
Debug Datasets
Datasets
ep32_chip_LA0
Design Hierarchy
ep32_chip
cpu1 (ep32_uniq_0)
gpio1 (gpio_uniq_0)
ram_memory_0(ram_mer
uart1 (uart_uniq_0)
aclk @Tc
arst @Tc
cpu_ack_o
cpu_addr_o[31:0] @T
cpu_byte0
cpu_byte1
cpu_byte2
Signal Search
Trigger Output Signal from Reveal
Trace Signal Setup
Trigger Signal Setup
Trace
arst
aclk
cpu1/code(6 bits)
memory_data_o(32 bits)
cpu_data_o(32 bits)
cpu_addr_o(32 bits)
Sample Clock
cpu1/clk
Implementation
Buffer Depth
256
Timestamp
Sample Enable
Sample Enable
Active High
Data Capture Mo
Single Trigg
Multiple Tri
Minimum samp
Include trigger signals in trace data
Message
Signal Information
Resource Usage
Loading Reveal project...
Ready

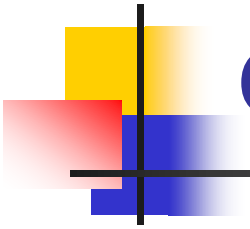

Reveal Logic Analyzer - [d:\isptool\demo_latticexp2_brevia_soc_vhdl\demo_latticexp...
File Bus/Signal Data Device Window Help
ep32_chip
Datasets
LFXP2-5E
ep32_c
Trace Bus/Signal
ep32_chip
arst
aclk
cpu1/c
memo
cpu_d
[Device0, ep32_chip_LA0] [Trace Bus Width: 104, Time St...
Stopped
0 Trigger Captured
Trigger Signal Setup
Waveform View
Trace Bus/...
arst
aclk
cpu1/cc
memor
cpu_da
cpu_ad
30
0:32
0:34
02
1E
0A
1D
0B
1E
0A74B05E
0A74B79E
80000002
020000CE
0000061B
00000000
00000041
80000002
00000041
000000D1
000000CE
000000CF
000000D0
80000002


Reveal Logic Analyzer - [d:\isptool\demo_latticexp2_brevia_soc_vhdl\demo_latticexp...
File
Bus/Signal
Data
Device
Window
Help
ep32_chip
[Device0, ep32_chip_LA0] [Trace Bus Width: 104, Time Stamp Widt...
Completed
1 Trigger Captured
Trigger Signal Setup
Waveform View
Trace Bus/...
30
0:32
0:34
0:36
arst
aclk
cpu1/cc
memor
cpu_da
cpu_ad
1E
00
1E
00
1E79E79E
00000020
0000061B
000007A8
00000000
00000000
00000001
00000002
00000020
Trace



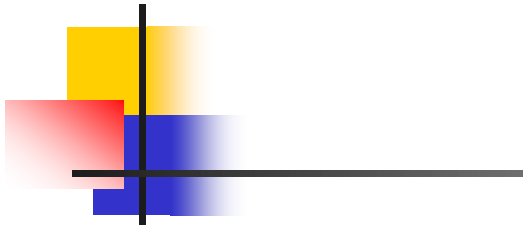
# Reveal eP32

- Very powerful debugging tool
- All signals in internal modules can be selected for tracing
- Waveform display is like a super-expansive logic analyzer
- It solved my reset problem in eP32.

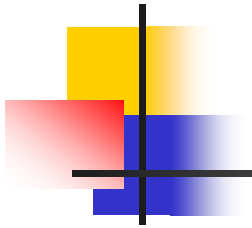


# eP32_xp2 Preliminary Release

- All VHDL design files
- All eForth metacompiler files
- weForth system files
- This book in ep32_xp2.pdf



# Questions?



# Thank You.