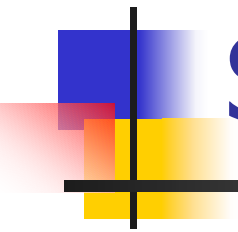


SPICE for the Complete Idiot

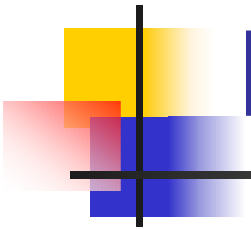
C. H. Ting
Silicon Valley FIG
4/30/2005

TRANSISTORS AND DIODES

- Junction Diodes
- Diode Model (D)
- Bipolar Junction Transistors (BJTs)
- BJT Models (NPN/PNP)
- Junction Field-Effect Transistors (JFETs)
- JFET Models (NJF/PJF)
- MOSFETs
- MOSFET Models (NMOS/PMOS)
- MESFETs
- MESFET Models (NMF/PMF)

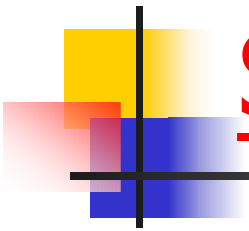
TYPES OF ANALYSIS

- DC Analysis
- AC Small-Signal Analysis
- Transient Analysis
- Pole-Zero Analysis
- Small-Signal Distortion Analysis
- Sensitivity Analysis
- Noise Analysis



Device Models

- R Semiconductor resistor model
- C Semiconductor capacitor model
- SW Voltage controlled switch
- D Diode model
- NPN NPN BJT model
- PNP PNP BJT model
- NMOS N-channel MOSFET model
- PMOS P-channel MOSFET model



SUBCIRCUITS

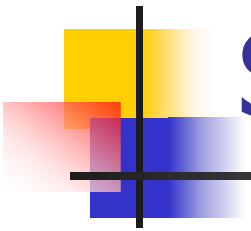
- .SUBCKT Line
- Subcircuit Calls
- Subcircuit Calls
- …
- .ENDS Line

VOLTAGE AND CURRENT SOURCES

- Independent Sources
  - Pulse
  - Sinusoidal
- Linear Dependent Sources
  - Linear Voltage-Controlled Current Sources
  - Linear Voltage-Controlled Voltage Sources
  - Linear Current-Controlled Current Sources
  - Linear Current-Controlled Voltage Sources
- Non-linear Dependent Sources

Spice for Logic Simulation

```
* Simulation of NAND gate
.control
destroy all
run
plot out1+30 out+24 set+18 clr+12 in1+6 in2
.endc
.tran 60p 100n 10p UIC
*x13 in1 in2 out NAND
.subckt NAND in1 in2 out
e1 out 0 value=if((v(in1)>2.5 && v(in2)>2.5), 0, 5)
.ends
end
```



Spice for Logic Simulation

- NAND
- NOR
- XOR
- INV
- TG
- DFF

Spice for Analog Circuits

- OpAmp

```
.subckt OPAMP in1 in2 out
e1 out 0 in1 in2 100000
.ends
```

- Comparator

```
.subckt COMPARE in1 in2 out
e1 out 0 value=if((v(in1)>v(in2)), 5, 0)
.ends
```

Spice for Analog Circuits

- Integrator

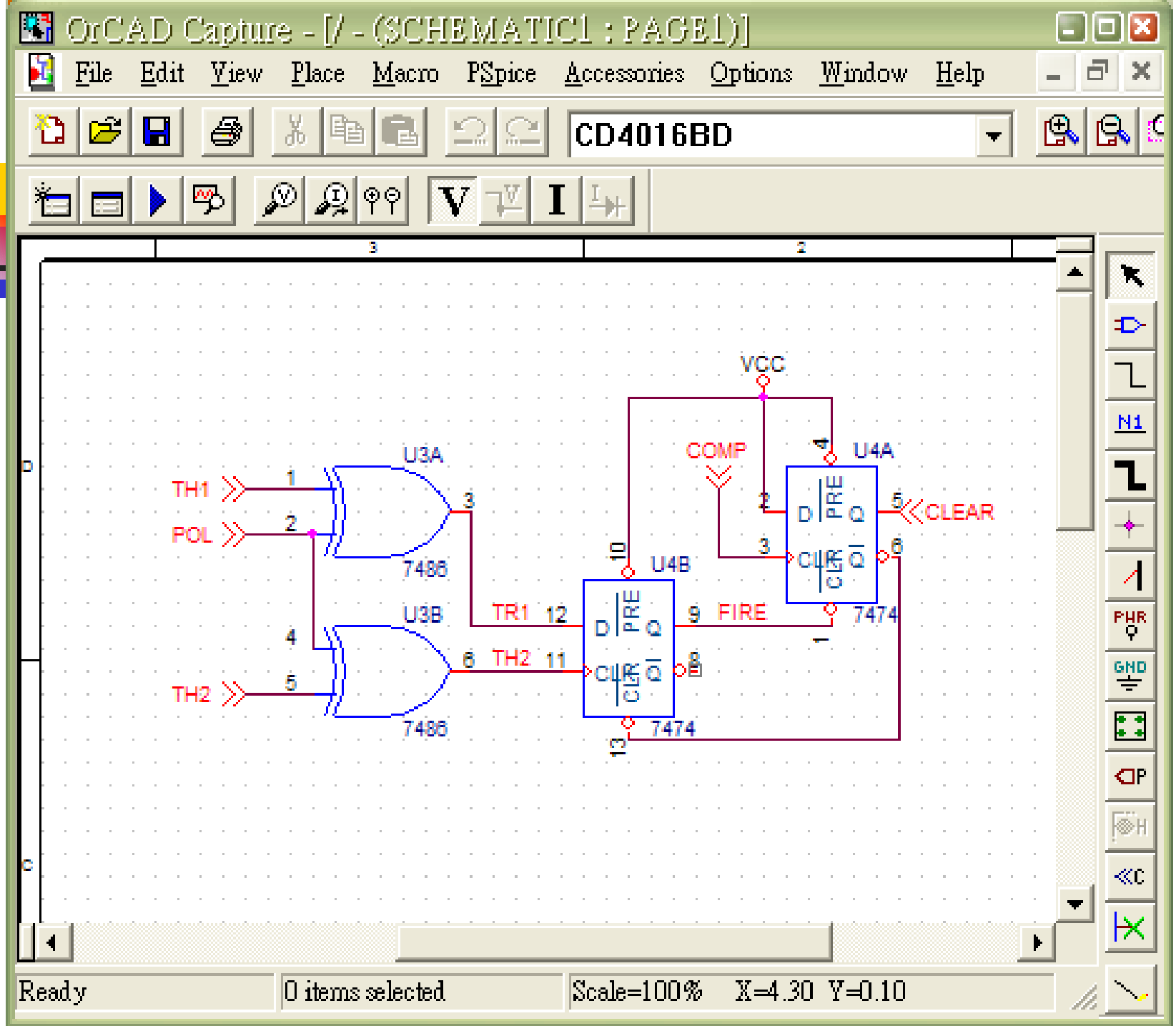
```
.subckt INTEGRATE in1 in2 out control
x1 in1 in out OPAMP
r1 in2 in 1k
r2 out in r=v(control)>1 ? 1meg : 50
c1 out in 5p
.ends
```

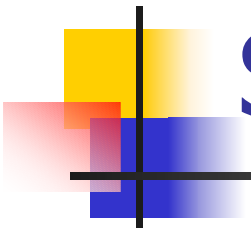
Spice for DSO Timebase

- Triggering unit
- Timebase unit

Spice of DSO Core Circuit

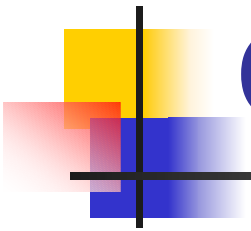
- Trigger Unit
  - 2 XOR
- Timebase Unit
  - 2 DFF for firing and clearing
- Schematics
- Spice source code
- Simulation wave forms


OrCAD Capture - [/ - (SCHEMATIC1 : PAGE1)]
File Edit View Place Macro PSpice Accessories Options Window Help
CD4016BD
VCC
COMP
U4A
U3A
U3B
U4B
TH1
POL
TH2
TR1
TH2
FIRE
CLEAR
7486
7486
7474
7474
PHR
GND
Ready
0 items selected
Scale=100%
X=4.30 Y=0.10



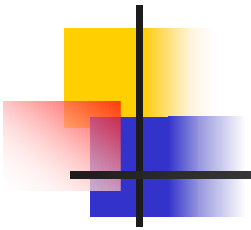
Spice of DSO Timebase

- Schematics
- Spice source code
- Simulation wave forms



Concluding Remarks

- WinSpice is very useful in logic simulation
- A simple template is very easy to adapt to many applications
- It allow us to consider building mixed signal ASIC chips



Thank you